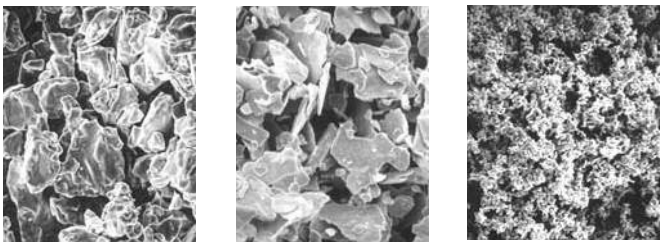
Section 4: Technical Summary and Application Guidelines

INTRODUCTION

Tantalum capacitors are manufactured from a powder of pure tantalum metal. OxiCap® - niobium oxide capacitor is made from niobium oxide NbO powder. The typical particle size is between 2 and 10 µm.

Figure below shows typical powders. Note the very great difference in particle size between the powder CVs/g.



4000µFV **20000µFV** **50000µFV**

Figure 1a. Tantalum powder

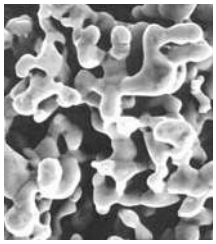


Figure 1b. Niobium Oxide powder

The powder is compressed under high pressure around a Tantalum or Niobium wire (known as the Riser Wire) to form a "pellet". The riser wire is the anode connection to the capacitor.

This is subsequently vacuum sintered at high temperature (typically 1200 - 1800°C) which produces a mechanically strong pellet and drives off any impurities within the powder.

During sintering the powder becomes a sponge like structure with all the particles interconnected in a huge lattice.

This structure is of high mechanical strength and density, but is also highly porous giving a large internal surface area (see Figure 2).

The larger the surface area the larger the capacitance. Thus high CV/g (capacitance voltage product per gram) powders, which have a low average particle size, are used for low voltage, high capacitance parts.

By choosing which powder and sinter temperature is used to produce each capacitance/voltage rating the surface area can be controlled.

The following example uses a 220µF 6V capacitor to illustrate the point.

$$C = \frac{\varepsilon_o \varepsilon_r A}{d}$$

where ε_o is the dielectric constant of free space (8.855×10^{-12} Farads/m)
ε_r is the relative dielectric constant
= 27 for Tantalum Pentoxide
= 41 for Niobium Pentoxide
d is the dielectric thickness in meters
C is the capacitance in Farads
and A is the surface area in meters

Rearranging this equation gives:

$$A = \frac{C d}{\varepsilon_o \varepsilon_r}$$

thus for a 220µF/6V capacitor the surface area is 346 square centimeters, or nearly a half times the size of this page.

The dielectric is then formed over all the Tantalum or niobium oxide surfaces by the electrochemical process of anodization. To activate this, the "pellet" is dipped into a very weak solution of phosphoric acid.

The dielectric thickness is controlled by the voltage applied during the forming process. Initially the power supply is kept in a constant current mode until the correct thickness of dielectric has been reached (that is the voltage reaches the 'forming voltage'), it then switches to constant voltage mode and the current decays to close to zero.

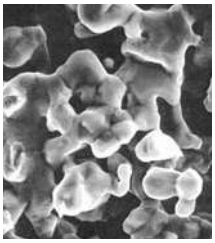


Figure 2. Sintered Anode

The chemical equations describing the process are as follows:

Tantalum Anode: $2\ Ta \rightarrow 2\ Ta^{5+} + 10\ e^-$

$2\ Ta^{5+} + 10\ OH^- \rightarrow Ta_2O_5 + 5\ H_2O$

Niobium Oxide Anode:

$2\ NbO \rightarrow 2\ NbO^{3+} + 6\ e^-$

$2\ NbO^{3+} + 6\ OH^- \rightarrow Nb_2O_5 + 3\ H_2O$

Cathode:

Tantalum: $10\ H_2O - 10\ e \rightarrow 5H_2 + 10\ OH^-$

Niobium Oxide: $6\ H_2O - 6\ e^- \rightarrow 3H_2 + 6\ OH^-$

The oxide forms on the surface of the Tantalum or Niobium Oxide but it also grows into the material. For each unit of oxide two thirds grows out and one third grows in. It is for this reason that there is a limit on the maximum voltage rating of Tantalum & Niobium Oxide capacitors with present technology powders (see Figure 3).

The dielectric operates under high electrical stress. Consider a 220µF 6V part:

Formation voltage = Formation Ratio x Working Voltage
= 3.5 x 6
= 21 Volts

Tantalum:
The pentoxide (Ta_2O_5) dielectric grows at a rate of 1.7×10^{-9} m/V

Dielectric thickness (d) = $21 \times 1.7 \times 10^{-9}$
= 0.036 µm

Electric Field strength = Working Voltage / d
= 167 KV/mm

Niobium Oxide:
The niobium oxide (Nb_2O_5) dielectric grows at a rate of 2.4×10^{-9} m/V

Dielectric thickness (d) = $21 \times 2.4 \times 10^{-9}$
= 0.050 µm

Electric Field strength = Working Voltage / d
= 120 KV/mm

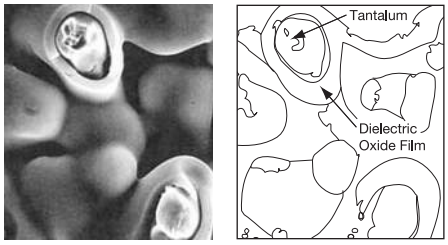


Figure 3. Dielectric layer

The next stage is the production of the cathode plate. This is achieved by pyrolysis of Manganese Nitrate into Manganese Dioxide.

The "pellet" is dipped into an aqueous solution of nitrate and then baked in an oven at approximately 250°C to produce the dioxide coat. The chemical equation is:

$$Mn(NO_3)_2 \rightarrow MnO_2 + 2NO_2$$

This process is repeated several times through varying specific densities of nitrate to build up a thick coat over all internal and external surfaces of the "pellet", as shown in Figure 4.

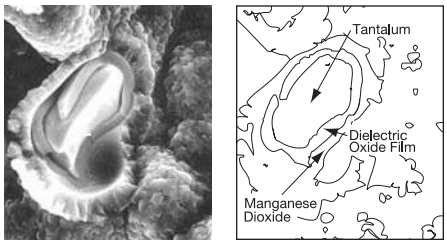


Figure 4. Manganese Dioxide Layer

The "pellet" is then dipped into graphite and silver to provide a good connection to the Manganese Dioxide cathode plate. Electrical contact is established by deposition of carbon onto the surface of the cathode. The carbon is then coated with a conductive material to facilitate connection to the cathode termination (see Figure 5). Packaging is carried out to meet individual specifications and customer requirements. This manufacturing technique is adhered to for the whole range of AVX Tantalum capacitors, which can be subdivided into four basic groups: Chip / Resin dipped / Rectangular boxed / Axial.

Further information on production of Tantalum Capacitors can be obtained from the technical paper "Basic Tantalum Technology", by John Gill, available from your local AVX representative.

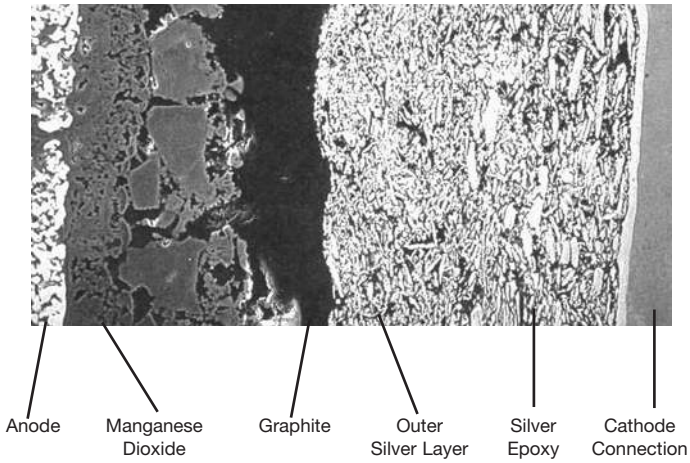


Figure 5. Cathode Termination

SECTION 1
ELECTRICAL CHARACTERISTICS AND EXPLANATION OF TERMS

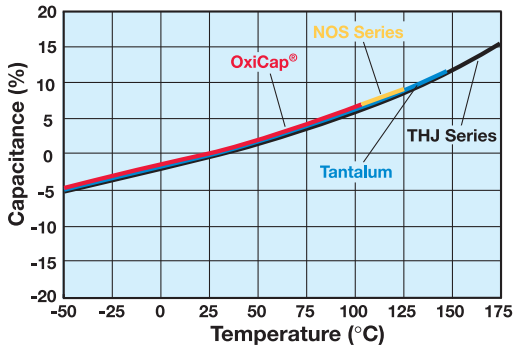
1.1 CAPACITANCE

1.1.1 Rated capacitance (C_R).
This is the nominal rated capacitance. For tantalum and OxiCap® capacitors it is measured as the capacitance of the equivalent series circuit at 25°C using a measuring bridge supplied by a 0.5V rms 120Hz sinusoidal signal, free of harmonics with a bias of 2.2Vd.c.

1.1.2 Capacitance tolerance.
This is the permissible variation of the actual value of the capacitance from the rated value. For additional reading, please consult the AVX technical publication "Capacitance Tolerances for Solid Tantalum Capacitors".

1.1.3 Temperature dependence of capacitance.
The capacitance of a tantalum capacitor varies with temperature. This variation itself is dependent to a small extent on the rated voltage and capacitor size.

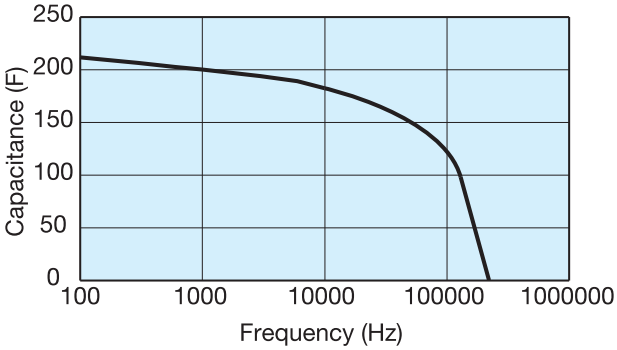
TYPICAL CAPACITANCE vs. TEMPERATURE



1.1.4 Frequency dependence of the capacitance.
The effective capacitance decreases as frequency increases. Beyond 100kHz the capacitance continues to drop until resonance is reached (typically between 0.5 - 5MHz depending on the rating). Beyond the resonant frequency the device becomes inductive.

TAJE227K010

CAPACITANCE vs. FREQUENCY



For individual part number please refer to SpiTan Software for frequency and temperature behavior found on AVX Corporation website.

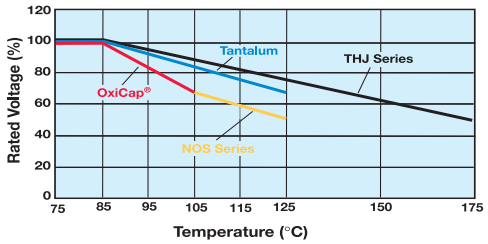
1.2 VOLTAGE

1.2.1 Rated d.c. voltage (V_R).
This is the rated d.c. voltage for continuous operation up to 85°C (up to 40°C for TLJ, TLN, NLJ series).

Operating voltage consists of the sum of DC bias voltage and ripple peak voltage. The peak voltage should not exceed the category voltage. For recommended voltage (application) derating refer to figure 2c of the SECTION 3.

1.2.2 Category voltage (V_C).
This is the maximum voltage that may be applied continuously to a capacitor. It is equal to the rated voltage up to +85°C (up to 40°C for TLJ, TLN, NLJ series), beyond which it is subject to a linear derating, to 2/3 V_R at 125°C for tantalum and 2/3 V_R at 105°C for OxiCap®.

MAXIMUM CATEGORY VOLTAGE vs. TEMPERATURE



1.2.3 Surge voltage (V_S).
This is the highest voltage that may be applied to a capacitor for short periods of time in circuits with minimum series resistance of 33Ohms (CECC states 1kΩ). The surge voltage may be applied up to 10 times in an hour for periods of up to 30 seconds at a time. The surge voltage must not be used as a parameter in the design of circuits in which, in the normal course of operation, the capacitor is periodically charged and discharged.

85°C Tantalum		125°C Tantalum*	
Rated Voltage V_R	Surge Voltage V_S	Category Voltage V_C	Surge Voltage V_S
2	2.7	1.3	1.7
2.5	3.3	1.7	2.2
3	3.9	2	2.6
4	5.2	2.7	3.4
5	6.5	3.3	4
6.3	8	4	5
10	13	7	8
16	20	10	13
20	26	13	16
25	32	17	20
35	46	23	28
50	65	33	40

85°C OxiCap®		105°C OxiCap®	
Rated Voltage V_R	Surge Voltage V_S	Category Voltage V_C	Surge Voltage V_S
1.8	2.3	1.2	1.6
2.5	3.3	1.7	2.2
4	5.2	2.7	3.4
6.3	8	4	5
10	13	7	8

*For THJ 175°C Category & Surge voltage see THJ section on pages 135-140.

1.2.4 Effect of surges

The solid Tantalum and OxiCap® capacitors have a limited ability to withstand voltage and current surges. This is in common with all other electrolytic capacitors and is due to the fact that they operate under very high electrical stress across the dielectric. For example a 6 volt tantalum capacitor has an Electrical Field of 167 kV/mm when operated at rated voltage. OxiCap® capacitors operate at electrical field significantly less than 167 kV/mm.

It is important to ensure that the voltage across the terminals of the capacitor never exceeds the specified surge voltage rating.

Solid tantalum capacitors and OxiCap® have a self healing ability provided by the Manganese Dioxide semiconducting layer used as the negative plate. However, this is limited in low impedance applications. In the case of low impedance circuits, the capacitor is likely to be stressed by current surges.

Derating the capacitor increases the reliability of the component. (See Figure 2b page 264). The "AVX Recommended Derating Table" (page 267) summarizes voltage rating for use on common voltage rails, in low impedance applications for both Tantalum and OxiCap® capacitors.

In circuits which undergo rapid charge or discharge a protective resistor of 1Ω/V is recommended. If this is impossible, a derating factor of up to 70% should be used on tantalum capacitors. OxiCap® capacitors can be used with derating of 20% minimum.

In such situations a higher voltage may be needed than is available as a single capacitor. A series combination should be used to increase the working voltage of the equivalent capacitor: For example, two 22µF 25V parts in series is equivalent to one 11µF 50V part. For further details refer to J.A. Gill's paper "Investigation into the Effects of Connecting Tantalum Capacitors in Series", available from AVX offices worldwide.

NOTE:
While testing a circuit (e.g. at ICT or functional) it is likely that the capacitors will be subjected to large voltage and current transients, which will not be seen in normal use. These conditions should be borne in mind when considering the capacitor's rated voltage for use. These can be controlled by ensuring a correct test resistance is used.

1.2.5 Reverse voltage and Non-Polar operation.

The values quoted are the maximum levels of reverse voltage which should appear on the capacitors at any time. These limits are based on the assumption that the capacitors are polarized in the correct direction for the majority of their working life. They are intended to cover short term reversals of polarity such as those occurring during switching transients of during a minor portion of an impressed waveform. Continuous application of reverse voltage without normal polarization will result in a degradation of leakage current. In conditions under which continuous application of a reverse voltage could occur two similar capacitors should be used in a back-to-back configuration with the negative terminations connected together. Under most conditions this combination will have a capacitance one half of the nominal capacitance of either capacitor. Under conditions of isolated pulses or during the first few cycles, the capacitance may approach the full nominal value. The reverse voltage ratings are designed to cover exceptional conditions of small level excursions into incorrect polarity. The values quoted are not intended to cover continuous reverse operation.

The peak reverse voltage applied to the capacitor must not exceed:

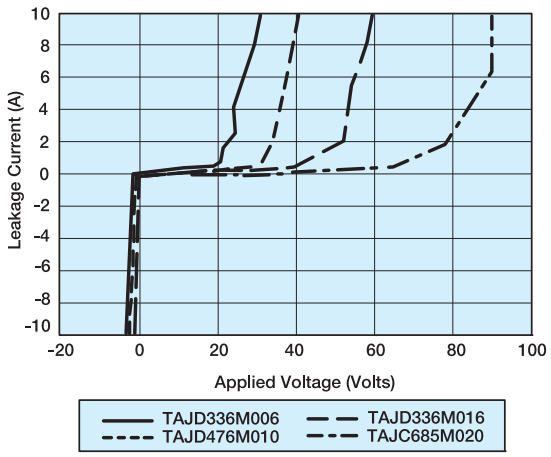
10% of the rated d.c. working voltage to a maximum of 1.0v at 25°C

3% of the rated d.c. working voltage to a maximum of 0.5v at 85°C

1% of the rated d.c. working voltage to a maximum of 0.1v at 125°C (0.1v at 150°C THJ Series)

Note: Capacitance and DF values of OxiCap® may exceed specification limits under these conditions.

LEAKAGE CURRENT vs. BIAS VOLTAGE



1.2.6 Superimposed A.C. Voltage (Vr.m.s.) - Ripple Voltage.

This is the maximum r.m.s. alternating voltage; superimposed on a d.c. voltage, that may be applied to a capacitor. The sum of the d.c. voltage and peak value of the superimposed a.c. voltage must not exceed the category voltage, v.c.

Full details are given in Section 2.

1.2.7 Forming voltage.

This is the voltage at which the anode oxide is formed. The thickness of this oxide layer is proportional to the formation voltage for a capacitor and is a factor in setting the rated voltage.

1.3 DISSIPATION FACTOR AND TANGENT OF LOSS ANGLE (TAN D)

1.3.1 Dissipation factor (D.F.).

Dissipation factor is the measurement of the tangent of the loss angle (tan δ) expressed as a percentage. The measurement of DF is carried out using a measuring bridge that supplies a 0.5V rms 120Hz sinusoidal signal, free of harmonics with a bias of 2.2Vdc. The value of DF is temperature and frequency dependent.

Note: For surface mounted products the maximum allowed DF values are indicated in the ratings table and it is important to note that these are the limits met by the component AFTER soldering onto the substrate.

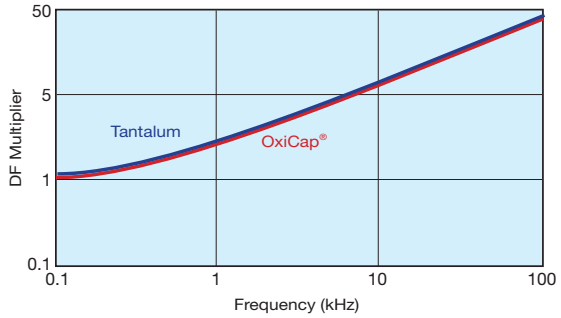
1.3.2 Tangent of Loss Angle (tan δ).

This is a measurement of the energy loss in the capacitor. It is expressed, as tan δ and is the power loss of the capacitor divided by its reactive power at a sinusoidal voltage of specified frequency. Terms also used are power factor, loss factor and dielectric loss. Cos (90 - δ) is the true power factor. The measurement of tan δ is carried out using a measuring bridge that supplies a 0.5V rms 120Hz sinusoidal signal, free of harmonics with a bias of 2.2Vdc.

1.3.3 Frequency dependence of Dissipation Factor.

Dissipation Factor increases with frequency as shown in the typical curves that are for tantalum and OxiCap® capacitors identical:

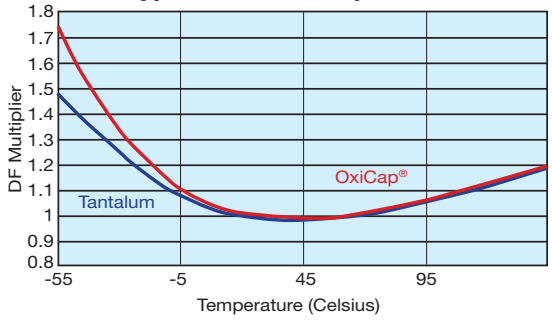
Typical DF vs Frequency



1.3.4 Temperature dependence of Dissipation Factor.

Dissipation factor varies with temperature as the typical curves show. These plots are identical for both Tantalum and OxiCap® capacitors. For maximum limits please refer to ratings tables.

Typical DF vs Temperature



1.4 IMPEDANCE, (Z) AND EQUIVALENT SERIES RESISTANCE (ESR)

1.4.1 Impedance, Z.

This is the ratio of voltage to current at a specified frequency. Three factors contribute to the impedance of a Tantalum capacitor; the resistance of the semiconductor layer; the capacitance value and the inductance of the electrodes and leads.

At high frequencies the inductance of the leads becomes a limiting factor. The temperature and frequency behavior of these three factors of impedance determine the behavior of the impedance Z. The impedance is measured at 25°C and 100kHz.

1.4.2 Equivalent Series Resistance, ESR.

Resistance losses occur in all practical forms of capacitors. These are made up from several different mechanisms, including resistance in components and contacts, viscous forces within the dielectric and defects producing bypass current paths. To express the effect of these losses they are considered as the ESR of the capacitor. The ESR is frequency dependent and can be found by using the relationship;

$$ESR = \frac{\tan \delta}{2\pi fC}$$

Where f is the frequency in Hz, and C is the capacitance in farads.

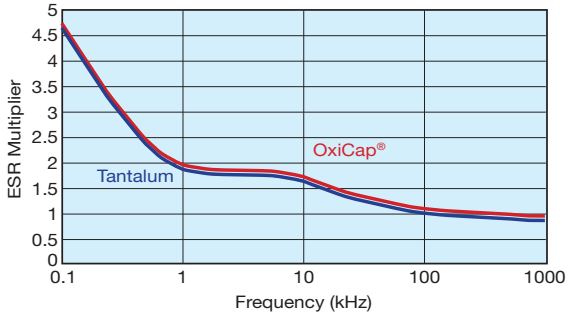
The ESR is measured at 25°C and 100kHz.

ESR is one of the contributing factors to impedance, and at high frequencies (100kHz and above) it becomes the dominant factor. Thus ESR and impedance become almost identical, impedance being only marginally higher.

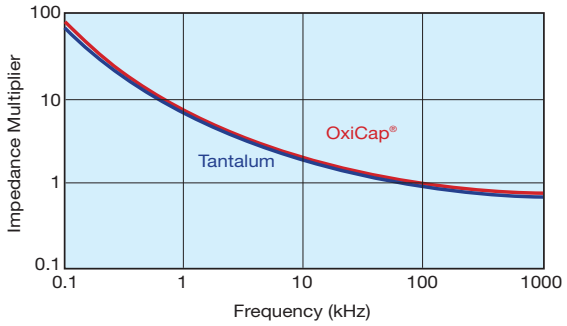
1.4.3 Frequency dependence of Impedance and ESR.

ESR and Impedance both increase with decreasing frequency. At lower frequencies the values diverge as the extra contributions to impedance (due to the reactance of the capacitor) become more significant. Beyond 1MHz (and beyond the resonant point of the capacitor) impedance again increases due to the inductance of the capacitor. Typical ESR and Impedance values are similar for both tantalum and niobium oxide materials and thus the same charts are valid for both for Tantalum and OxiCap® capacitors.

Typical ESR vs Frequency



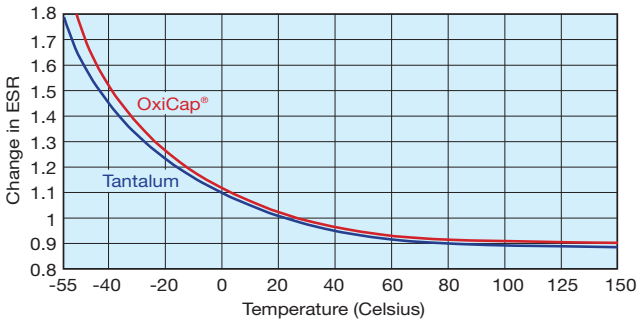
Typical Impedance vs Frequency



1.4.4 Temperature dependence of the Impedance and ESR.

At 100kHz, impedance and ESR behave identically and decrease with increasing temperature as the typical curves show.

Typical 100kHz ESR vs Temperature



1.5 D.C. LEAKAGE CURRENT

1.5.1 Leakage current.

The leakage current is dependent on the voltage applied, the elapsed time since the voltage was applied and the component temperature. It is measured at +20°C with the rated voltage applied. A protective resistance of 1000Ω is connected in series with the capacitor in the measuring circuit. Three to five minutes after application of the rated voltage the leakage current must not exceed the maximum values indicated in the ratings table. Leakage current is referenced as DCL (for Direct Current Leakage). The default maximum limit for DCL Current is given by DCL = 0.01CV, where DCL is in microamperes, and C is the capacitance rating in microfarads, and V is the voltage rating in volts. DCL of tantalum capacitors vary within arrange of 0.01 - 0.1CV or 0.5µA (whichever is the greater). And 0.02 - 0.1CV or 1.0µA (whichever is the greater) for OxiCap® capacitors.

Reforming of Tantalum or OxiCap® capacitors is unnecessary even after prolonged storage periods without the application of voltage.

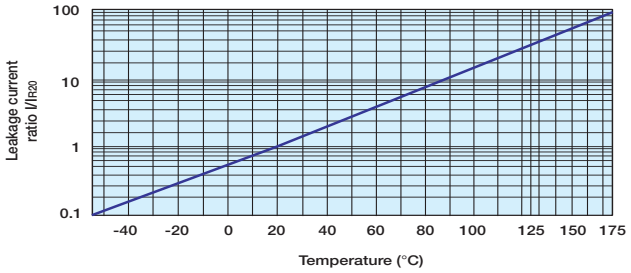
1.5.2 Temperature dependence of the leakage current.

The leakage current increases with higher temperatures; typical values are shown in the graph. For operation between 85°C and 125°C, the maximum working voltage must be derated and can be found from the following formula.

$$V_{max} = \left(1 - \frac{(T - 85)}{125}\right) \times V_R$$

where T is the required operating temperature.

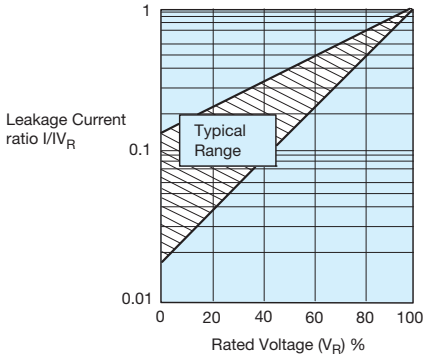
LEAKAGE CURRENT vs. TEMPERATURE



1.5.3 Voltage dependence of the leakage current.

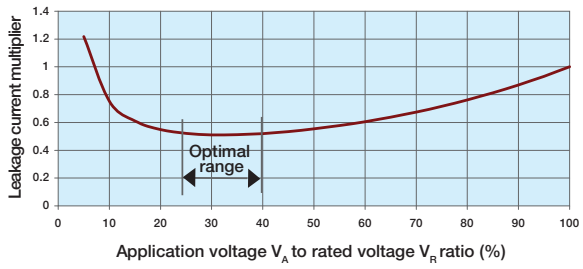
The leakage current drops rapidly below the value corresponding to the rated voltage V_R when reduced voltages are applied. The effect of voltage derating on the leakage current is shown in the graph. This will also give a significant increase in the reliability for any application. See Section 3.1 (page 264) for details.

LEAKAGE CURRENT vs. RATED VOLTAGE



For input condition of fixed application voltage and including median curve of the Leakage current vs. Rated voltage graph displayed above we can evaluate following curve.

LEAKAGE CURRENT MULTIPLIER **vs.** VOLTAGE DERATING
for FIXED APPLICATION VOLTAGE V_A



We can identify the range of V_A/V_R (derating) values with minimum actual DCL as the "optimal" range. Therefore the minimum DCL is obtained when capacitor is used at 25 to 40 % of rated voltage - when the rated voltage of the capacitor is 2.5 to 4 times higher than actual application voltage.

For additional information on Leakage Current, please consult the AVX technical publication "Analysis of Solid Tantalum Capacitor Leakage Current" by R. W. Franklin.

1.5.4 Ripple current.

The maximum ripple current allowed is derived from the power dissipation limits for a given temperature rise above ambient temperature (please refer to Section 2, pages 261-262).

1.6 SELF INDUCTANCE (ESL)

The self-inductance value (ESL) can be important for resonance frequency evaluation. See figure below typical ESL values per case size.

TAJ/TMJ/TPS/TRJ/THJ/TLJ/TCJ/TCQ/ NLJ/NOJ/NOS

Case Size	Typical Self Inductance value (nH)	Case Size	Typical Self Inductance value (nH)	Case Size	Typical Self Inductance value (nH)
A	1.8	H	1.8	U	2.4
B	1.8	K	1.8	V	2.4
C	2.2	N	1.4	W	2.2
D	2.4	P	1.4	X	2.4
E	2.5	R	1.4	Y	2.4
F	2.2	S	1.8	5	2.4
G	1.8	T	1.8		

TAC/TLC/TPC

Case Size	Typical Self-Inductance value (nH)
A	1.5
B	1.6
D	1.4
E	1.0
H	1.4
I	1.3
J	1.2
K	1.1
L	1.2
M	1.3
R	1.4
T	1.6
U	1.3
V	1.5
Z	1.1

TCM/TPM TRM/NOM

Case Size	Typical Self-Inductance value (nH)
D	1.0
E	2.5
U	2.4
V	2.4
Y	1.0

TLN/TCN/J-CAP™

Case Size	Typical Self-Inductance value (nH)
K	1.0
L	1.0
M	1.3
N	1.3
O	1.0
S	1.0
T	1.0
X	1.8
3	2.0
4	2.2
6	2.5

SECTION 2
A.C. OPERATION, RIPPLE VOLTAGE AND RIPPLE CURRENT

2.1 RIPPLE RATINGS (A.C.)

In an a.c. application heat is generated within the capacitor by both the a.c. component of the signal (which will depend upon the signal form, amplitude and frequency), and by the d.c. leakage. For practical purposes the second factor is insignificant. The actual power dissipated in the capacitor is calculated using the formula:

$$P = I^2 R$$

and rearranged to $I = SQRT (P/R)$ .....(Eq. 1)

where I = rms ripple current, amperes
R = equivalent series resistance, ohms
U = rms ripple voltage, volts
P = power dissipated, watts
Z = impedance, ohms, at frequency under consideration

Maximum a.c. ripple voltage (U_{max}).

From the Ohms' law equation:

$U_{max} = IR$ .....(Eq. 2)

Where P is the maximum permissible power dissipated as listed for the product under consideration (see tables).

However care must be taken to ensure that:

1. The d.c. working voltage of the capacitor must not be exceeded by the sum of the positive peak of the applied a.c. voltage and the d.c. bias voltage.

2. The sum of the applied d.c. bias voltage and the negative peak of the a.c. voltage must not allow a voltage reversal in excess of the "Reverse Voltage".

Historical ripple calculations.
Previous ripple current and voltage values were calculated using an empirically derived power dissipation required to give a 10°C (30°C for polymer) rise of the capacitors body temperature from room temperature, usually in free air. These values are shown in Table I. Equation 1 then allows the maximum ripple current to be established, and Equation 2, the maximum ripple voltage. But as has been shown in the AVX article on thermal management by I. Salisbury, the thermal conductivity of a Tantalum chip capacitor varies considerably depending upon how it is mounted.

Table I: Power Dissipation Ratings (In Free Air)

TAJ/TMJ/TPS/TPM/TRJ/TRM/THJ/TLJ/TLN/TCJ/TCM/TCN/J-CAP™/TCQ/NLJ/NOJ/NOS/NOM Series Molded Chip

	Max. power dissipation (W)						
	Tantalum			Polymer		OxiCap®	
Case Size	TAJ/TMJ/TPS TRJ/THJ TLJ	TLN	TPM TRM	TCJ TCN J-CAP™ TCQ	TCM	NLJ NOJ NOS	NOM
A	0.075	—	—	0.100	—	0.090	—
B	0.085	—	—	0.125	—	0.102	—
C	0.110	—	—	0.175	—	0.132	—
D	0.150	—	0.255	0.225	–	0.180	—
E	0.165	—	0.270	0.250	0.410	0.198	0.324
F	0.100	—	—	0.150	—	0.120	—
G	0.070	0.060	—	0.100	—	0.084	—
H	0.080	0.070	—	0.100	—	0.096	—
K	0.065	0.055	—	0.090	—	0.078	—
L	0.070	0.060	—	0.095	—	0.084	—
M	—	0.040	—	0.080	—	—	—
N	0.050	0.040	—	0.080	—	—	—
O	–	–	—	0.065	—	—	—
P	0.060	—	—	0.090	—	0.072	—
R	0.055	—	—	0.085	—	0.066	—
S	0.065	0.055	—	0.095	—	0.078	—
T	0.080	0.070	—	0.100	—	0.096	—
U	0.165	—	0.295	0.380	—	—	—
V	0.250	—	0.285	0.360	0.420	0.300	—
W	0.090	—	—	0.130	—	0.108	—
X	0.100	—	—	0.175	—	0.120	—
Y	0.125	0.115	0.210	0.185	–	0.150	—
3	—	—	—	0.145	—	—	—
4	—	0.165	—	0.190	—	—	—
5	—	—	—	0.240	—	—	—
6	—	0.230	—	—	—	—	—

TACmicrochip® Series

Case Size	Max. power dissipation (W)
A	0.040
B	0.040
D	0.035
E	0.010
H	0.040
I	0.035
J	0.020
K	0.015
L	0.025
M	0.030
Q	0.040
R	0.045
T	0.040
U	0.035
V	0.035
X	0.040
Z	0.020

NLJ/NOJ/NOS/NOM

Temperature correction factor for ripple current	
Temp. °C	Factor
+25	1.00
+55	0.95
+85	0.90
+105	0.40
+125 (NOS,NOM)	0.40

TAJ/TPS/TPM/TRJ/TRM/THJ/TLJ/TLN

Temp °C	Correction Factor for ripple current	Correction Factor for Power Dissipation	Max. Temperature rise °C
up to 25°C	1.00	1.00	10
+55	0.95	0.90	9
+85	0.90	0.81	8.1
+105	0.65	0.42	4.2
+115	0.49	0.24	2.4
+125	0.40	0.16	1.6
+175 (THJ)	0.20	0.04	0.4
+200 (THJ)	0.10	0.01	0.1

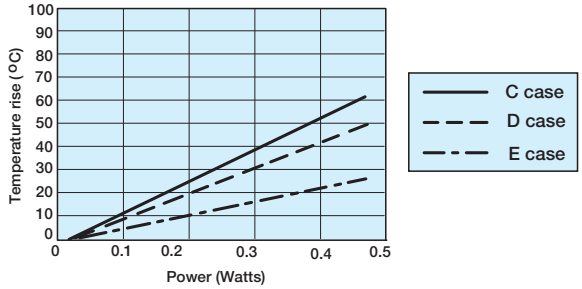
TCJ/TCM/TCN/J-CAP™/TCQ

Temp °C	Correction Factor for ripple current	Correction Factor for Power Dissipation	Max. Temperature rise °C
up to 45°C	1.00	1.00	30
+85	0.70	0.49	15
+105	0.45	0.20	6
+125	0.25	0.06	1.8

Technical Summary and Application Guidelines

A piece of equipment was designed which would pass sine and square wave currents of varying amplitudes through a biased capacitor. The temperature rise seen on the body for the capacitor was then measured using an infra-red probe. This ensured that there was no heat loss through any thermo-couple attached to the capacitor's surface.

Results for the C, D and E case sizes



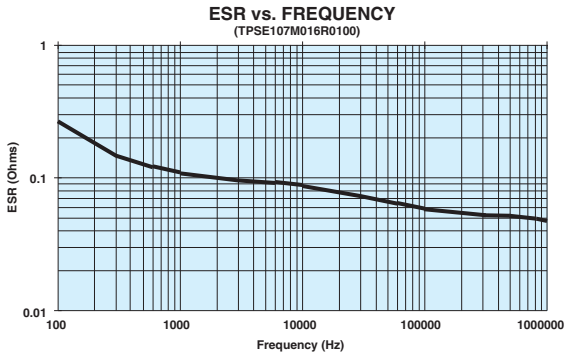
Several capacitors were tested and the combined results are shown above. All these capacitors were measured on FR4 board, with no other heat sinking. The ripple was supplied at various frequencies from 1kHz to 1MHz.

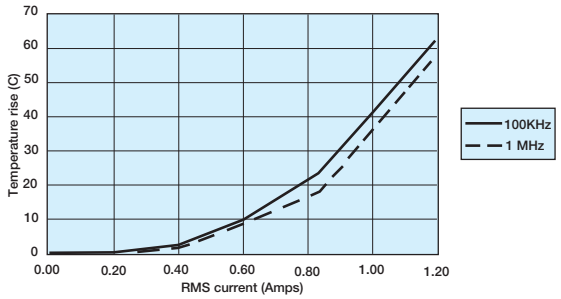
As can be seen in the figure above, the average P_{max} value for the C case capacitors was 0.11 Watts. This is the same as that quoted in Table I.

The D case capacitors gave an average P_{max} value 0.125 Watts. This is lower than the value quoted in the Table I by 0.025 Watts. The E case capacitors gave an average P_{max} of 0.200 Watts that was much higher than the 0.165 Watts from Table I.

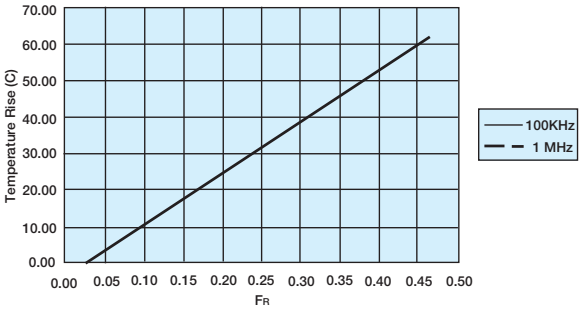
If a typical capacitor's ESR with frequency is considered, e.g. figure below, it can be seen that there is variation. Thus for a set ripple current, the amount of power to be dissipated by the capacitor will vary with frequency. This is clearly shown in figure in top of next column, which shows that the surface temperature of the unit raises less for a given value of ripple current at 1MHz than at 100kHz.

The graph below shows a typical ESR variation with frequency. Typical ripple current versus temperature rise for 100kHz and 1MHz sine wave inputs.





If I^2R is then plotted it can be seen that the two lines are in fact coincident, as shown in figure below.



Example

A Tantalum capacitor is being used in a filtering application, where it will be required to handle a 2 Amp peak-to-peak, 200kHz square wave current.

A square wave is the sum of an infinite series of sine waves at all the odd harmonics of the square waves fundamental frequency. The equation which relates is:

$I_{Square} = I_{pk}\sin(2\pi f) + I_{pk}\sin(6\pi f) + I_{pk}\sin(10\pi f) + I_{pk}\sin(14\pi f) + \ldots$

Thus the special components are:

Frequency	Peak-to-peak current (Amps)	RMS current (Amps)
200 KHz	2.000	0.707
600 KHz	0.667	0.236
1 MHz	0.400	0.141
1.4 MHz	0.286	0.101

Let us assume the capacitor is a TAJD686M006
Typical ESR measurements would yield.

Frequency	Typical ESR (Ohms)	Power (Watts) $Irms^2$ x ESR
200 KHz	0.120	0.060
600 KHz	0.115	0.006
1 MHz	0.090	0.002
1.4 MHz	0.100	0.001

Thus the total power dissipation would be 0.069 Watts.

From the D case results shown in figure top of previous column, it can be seen that this power would cause the capacitors surface temperature to rise by about 5°C. For additional information, please refer to the AVX technical publication "Ripple Rating of Tantalum Chip Capacitors" by R.W. Franklin.

2.2 OxiCap® RIPPLE RATING

OxiCap® capacitors showing 20% higher power dissipation allowed compared to tantalum capacitors as a result of twice higher specific heat of niobium oxide compared to Tantalum powders. (Specific heat is related to energy necessary to heat a defined volume of material to a specified temperature.)

2.3 THERMAL MANAGEMENT

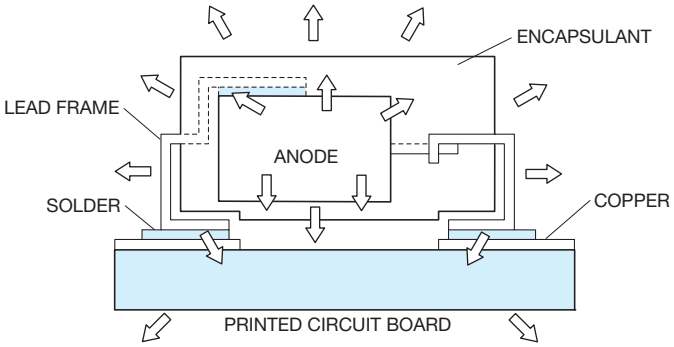
The heat generated inside a tantalum capacitor in a.c. operation comes from the power dissipation due to ripple current. It is equal to I^2R, where I is the rms value of the current at a given frequency, and R is the ESR at the same frequency with an additional contribution due to the leakage current. The heat will be transferred from the outer surface by conduction. How efficiently it is transferred from this point is dependent on the thermal management of the board.

The power dissipation ratings given in Section 2.1 (page 235) are based on free-air calculations. These ratings can be approached if efficient heat sinking and/or forced cooling is used.

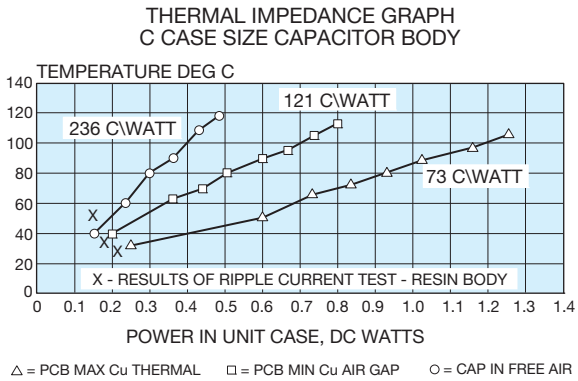
In practice, in a high density assembly with no specific thermal management, the power dissipation required to give a 10°C (30°C for polymer) rise above ambient may be up to a factor of 10 less. In these cases, the actual capacitor temperature should be established (either by thermocouple probe or infra-red scanner) and if it is seen to be above this limit it may be necessary to specify a lower ESR part or a higher voltage rating.

Please contact application engineering for details or contact the AVX technical publication entitled “Thermal Management of Surface Mounted Tantalum Capacitors” by Ian Salisbury.

Thermal Dissipation from the Mounted Chip



Thermal Impedance Graph with Ripple Current

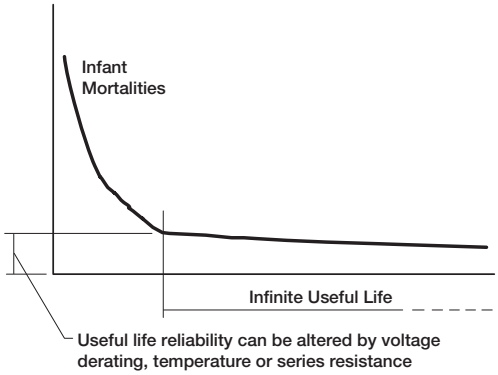


SECTION 3
RELIABILITY AND CALCULATION OF FAILURE RATE

3.1 STEADY-STATE

Both Tantalum and Niobium Oxide dielectric have essentially no wear out mechanism and in certain circumstances is capable of limited self healing. However, random failures can occur in operation. The failure rate of Tantalum capacitors will decrease with time and not increase as with other electrolytic capacitors and other electronic components.

Figure 1. Tantalum and OxiCap® Reliability Curve



The useful life reliability of the Tantalum and OxiCap® capacitors in steady-state is affected by three factors. The equation from which the failure rate can be calculated is:

$$F = F_V \times F_T \times F_R \times F_B$$

where F_V is a correction factor due to operating voltage/voltage derating

F_T is a correction factor due to operating temperature

F_R is a correction factor due to circuit series resistance

F_B is the basic failure rate level

Base failure rate.

Standard Tantalum conforms to Level M reliability (i.e. 1%/1000 hrs) or better at rated voltage, 85°C and 0.1Ω/volt circuit impedance.

F_B = 1.0% / 1000 hours for TAJ, TPS, TPM, TCJ, TCQ, TCM, TCN, J-CAP™, TAC

0.5% / 1000 hours for TMJ, TRJ, TRM, THJ & NOJ

0.2% / 1000 hours for NOS and NOM

TLJ, TLN, TLC and NLJ series of tantalum capacitors are defined at 0.5 x rated voltage at 85°C due to the temperature derating.

F_B = 0.2%/1000 hours at 85°C and 0.5xV_R with 0.1Ω/V series impedance with 60% confidence level.

Operating voltage/voltage derating.

If a capacitor with a higher voltage rating than the maximum line voltage is used, then the operating reliability will be improved. This is known as voltage derating.

The graph, Figure 2a, shows the relationship between voltage derating (the ratio between applied and rated voltage) and the failure rate. The graph gives the correction factor FU for any operating voltage.

Figure 2a. Correction factor to failure rate F_V for voltage derating of a typical component (60% con. level).

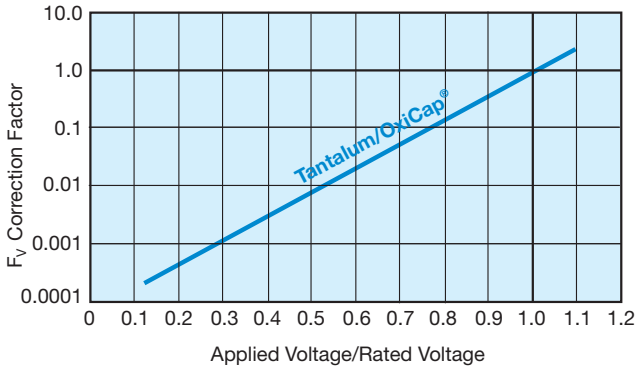


Figure 2b. Gives our recommendation for voltage derating for tantalum capacitors to be used in typical applications.

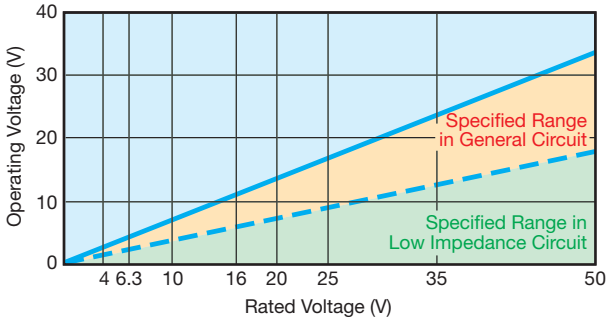
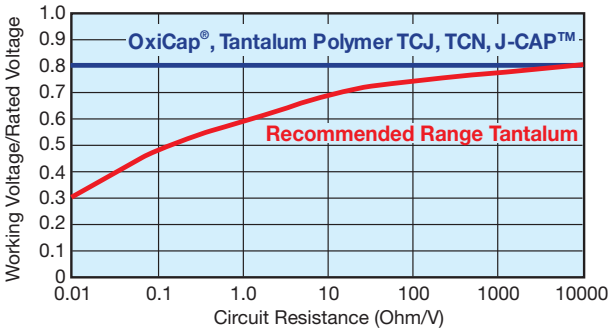


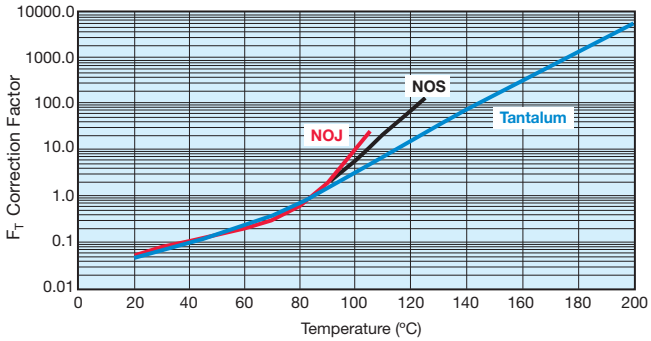
Figure 2c. Gives voltage derating recommendations for tantalum capacitors as a function of circuit impedance.



Operating Temperature.

If the operating temperature is below the rated temperature for the capacitor then the operating reliability will be improved as shown in Figure 3. This graph gives a correction factor F_T for any temperature of operation.

Figure 3: Correction factor to failure rate F_R for ambient temperature T for typical component (60% con. level).



Circuit Impedance.

All solid Tantalum and/or niobium oxide capacitors require current limiting resistance to protect the dielectric from surges. A series resistor is recommended for this purpose. A lower circuit impedance may cause an increase in failure rate, especially at temperatures higher than 20°C. An inductive low impedance circuit may apply voltage surges to the capacitor and similarly a non-inductive circuit may apply current surges to the capacitor, causing localized over-heating and failure. The recommended impedance is 1 Ω per volt. Where this is not feasible, equivalent voltage derating should be used (See MIL HANDBOOK 217). The graph, Figure 4, shows the correction factor, F_R, for increasing series resistance.

Figure 4. Correction factor to failure rate F_R for series resistance R on basic failure rate F_B for a typical component (60% con. level).

Circuit resistance ohms/volt	F_R
3.0	0.07
2.0	0.1
1.0	0.2
0.8	0.3
0.6	0.4
0.4	0.6
0.2	0.8
0.1	1.0

For circuit impedances below 0.1 ohms per volt, or for any mission critical application, circuit protection should be considered. An ideal solution would be to employ an AVX SMT thin-film fuse in series.

Example calculation.

Consider a 12 volt power line. The designer needs about 10µF of capacitance to act as a decoupling capacitor near a video bandwidth amplifier. Thus the circuit impedance will be limited only by the output impedance of the board's power unit and the track resistance. Let us assume it to be about 2 Ohms minimum, i.e. 0.167 Ohms/Volt. The operating temperature range is -25°C to +85°C.

If a 10µF 16 Volt capacitor was designed in the operating failure rate would be as follows.

a) F_T = 1.0 @ 85°C
b) F_R = 0.85 @ 0.167 Ohms/Volt
c) F_V = 0.08 @ applied voltage/rated voltage = 75%
d) F_B = 1%/1000 hours, basic failure rate level

Thus F = 1.0 x 0.85 x 0.08 x 1 = 0.068%/1000 Hours

If the capacitor was changed for a 20 volt capacitor, the operating failure rate will change as shown.

F_V = 0.018 @ applied voltage/rated voltage = 60%
F = 1.0 x 0.85 x 0.018 x 1 = 0.0153%/1000 Hours

3.2 Dynamic.

As stated in Section 1.2.4 (page 257), the solid capacitor has a limited ability to withstand voltage and current surges. Such current surges can cause a capacitor to fail. The expected failure rate cannot be calculated by a simple formula as in the case of steady-state reliability. The two parameters under the control of the circuit design engineer known to reduce the incidence of failures are derating and series resistance.

The table below summarizes the results of trials carried out at AVX with a piece of equipment, which has very low series resistance with no voltage derating applied. That is if the capacitor was tested at its rated voltage. It has been tested on tantalum capacitors, however the conclusions are valid for both tantalum and OxiCap® capacitors.

Results of production scale derating experiment

Capacitance and Voltage	Number of units tested	50% derating applied	No derating applied
47µF 16V	1,547,587	0.03%	1.1%
100µF 10V	632,876	0.01%	0.5%
22µF 25V	2,256,258	0.05%	0.3%

As can clearly be seen from the results of this experiment, the more derating applied by the user, the less likely the probability of a surge failure occurring.

It must be remembered that these results were derived from a highly accelerated surge test machine, and failure rates in the low ppm are more likely with the end customer.

A commonly held misconception is that the leakage current of a Tantalum capacitor can predict the number of failures which will be seen on a surge screen. This can be disproved by the results of an experiment carried out at AVX on 47µF

10V surface mount capacitors with different leakage currents. The results are summarized in the table below.

Leakage current vs number of surge failures.

Again, it must be remembered that these results were derived from a highly accelerated surge test machine, and failure rates in the low ppm are more likely with the end customer.

	Number tested	Number failed surge
Standard leakage range 0.1 µA to 1µA	10,000	25
Over Catalog limit 5µA to 50µA	10,000	26
Classified Short Circuit 50µA to 500µA	10,000	25

OxiCap® capacitor is less sensitive to an overloading stress compared to Tantalum and so a 20% minimum derating is recommended. It may be necessary in extreme low impedance circuits of high transient or 'switch-on' currents to derate the voltage further. Hence in general a lower voltage OxiCap® part number can be placed on a higher rail voltage compared to the tantalum capacitor – see table below.

AVX recommended derating table.

Voltage Rail (V)	Rated Voltage of Cap (V)	
	Tantalum	OxiCap®
3.3	6.3	4
5	10	6.3
8	16	10
10	20	–
12	25	–
15	35	–
>24	Series Combination	–

For further details on surge in Tantalum capacitors refer to J.A. Gill's paper "Surge in Solid Tantalum Capacitors", available from AVX offices worldwide.

An added bonus of increasing the derating applied in a circuit, to improve the ability of the capacitor to withstand surge conditions, is that the steady-state reliability is improved by up to an order. Consider the example of a 6.3 volt capacitor being used on a 5 volt rail.

The steady-state reliability of a Tantalum capacitor is affected by three parameters; temperature, series resistance and voltage derating. Assume 40°C operation and 0.1 Ohms/Volt series resistance.

The capacitors reliability will therefore be:

$$\text{Failure rate} = F_U \times F_T \times F_R \times 1\%/1000 \text{ hours}$$
$$= 0.15 \times 0.1 \times 1 \times 1\%/1000 \text{ hours}$$
$$= 0.015\%/1000 \text{ hours}$$

If a 10 volt capacitor was used instead, the new scaling factor would be 0.006, thus the steady-state reliability would be:

$$\text{Failure rate} = F_U \times F_T \times F_R \times 1\%/1000 \text{ hours}$$
$$= 0.006 \times 0.1 \times 1 \times 1\%/1000 \text{ hours}$$
$$= 6 \times 10^{-4} \%/1000 \text{ hours}$$

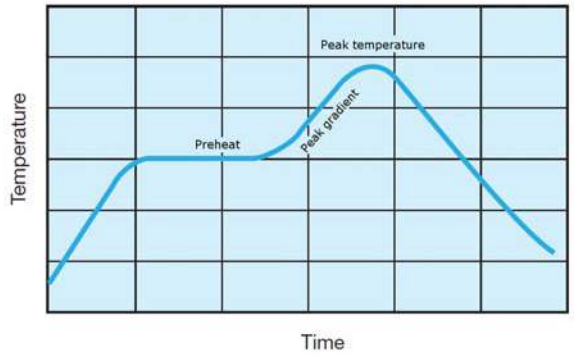
So there is an order improvement in the capacitors steady-state reliability.

SECTION 4
RECOMMENDED SOLDERING CONDITIONS

Both Tantalum and OxiCap® are lead-free system compatible components, meeting requirements of J-STD-020 standard. The maximum conditions with care: Max. Peak Temperature: 260ºC for maximum 10s, 3 reflow cycles. 2 cycles are allowed for F-series capacitors.

Small parametric shifts may be noted immediately after reflow, components should be allowed to stabilize at room temperature prior to electrical testing.

RECOMMENDED REFLOW PROFILE



Lead-free soldering:

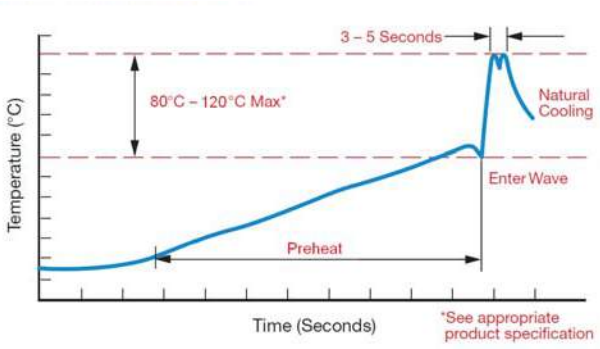
Pre-heating: 150±15ºC/60–120sec.
Max. Peak Temperature: 245±5ºC
Max. Peak Temperature Gradient: 2.5ºC/sec.
Max. Time above 230ºC: 40sec. max.

SnPb soldering:

Pre-heating: 150±15ºC/60–90sec.
Max. Peak Temperature: 220±5ºC
Max. Peak Temperature Gradient: 2ºC/sec.
Max. Time above solder melting point: 60sec.

RECOMMENDED WAVE SOLDERING

Lead-free soldering:



Pre-heating: 50-165ºC/90-120sec.
Max. Peak Temperature: 250-260ºC
Time of wave: 3-5sec.(max. 10sec.)

SnPb soldering:

Pre-heating: 50-165ºC/90–120sec.
Max. Peak Temperature: 240-250ºC
Time of wave: 3-5sec.(max.10sec.)

The upper side temperature of the board should not exceed +150ºC.

GENERAL LEAD-FREE NOTES

The following should be noted by customers changing from lead based systems to the new lead free pastes.

a) The visual standards used for evaluation of solder joints will need to be modified as lead-free joints are not as bright as with tin-lead pastes and the fillet may not be as large.

b) Resin color may darken slightly due to the increase in temperature required for the new pastes.

c) Lead-free solder pastes do not allow the same self alignment as lead containing systems. Standard mounting pads are acceptable, but machine set up may need to be modified.

Note: TCJ, TCM, TCN, J-CAP™, TCQ, F38, F39, TLN and F98 series are not dedicated to wave soldering.

RECOMMENDED HAND SOLDERING

Recommended hand soldering condition:

Tip Diameter	Selected to fit Application
Max. Tip Temperature	+370°C
Max. Exposure Time	3s
Anti-static Protection	Non required

Note: TCJ, TCM, TCN, J-CAP™, TCQ, F38, F39, TLN and F98 series are not dedicated to hand soldering.

SECTION 5
TERMINATIONS

5.1 Basic Materials

Two basic materials are used for termination leads: Nilo 42 (Fe58Ni42) and copper. Copper lead frame is mainly used for products requiring low ESR performance, while Nilo 42 is used for other products. The actual status of basic material per individual part type can be checked with AVX.

5.2 Termination Finishes – Coatings

Three terminations plating are available. Standard plating material is pure matte tin (Sn). Gold or tin-lead (SnPb) are available upon request with different part number suffix designations.*

5.2.1. Pure matte tin is used as the standard coating material meeting lead-free and RoHS requirements. AVX carefully monitors the latest findings on prevention of whisker formation. Currently used techniques include use of matte tin electrodeposition, nickel barrier underplating and recrystallization of surface by reflow. Terminations are tested for whiskers according to NEMI recommendations and JEDEC standard requirements. Data is available upon request.

5.2.2. Gold Plating is available as a special option* mainly for hybrid assembly using conductive glue.

5.2.3. Tin-lead (90%Sn 10%Pb) electroplated termination finish is available as a special option* upon request.

* Some plating options can be limited to specific part types. Please check availability of special options with AVX.

SECTION 6
MECHANICAL AND THERMAL PROPERTIES OF CAPACITORS

6.1 Acceleration
98.1m/s² (10g)

6.2 Vibration Severity
10 to 2000Hz, 0.75mm of 98.1m/s² (10g)

6.3 Shock
Trapezoidal Pulse, 98.1m/s² for 6ms.

6.4 Adhesion to Substrate
IEC 384-3. minimum of 5N.

6.5 Resistance to Substrate Bending
The component has compliant leads which reduces the risk of stress on the capacitor due to substrate bending.

6.6 Soldering Conditions
Dip soldering is permissible provided the solder bath temperature is ≤ 270°C, the solder time < 3 seconds and the circuit board thickness ≥ 1.0mm.

6.7 Installation Instructions
The upper temperature limit (maximum capacitor surface temperature) must not be exceeded even under the most unfavorable conditions when the capacitor is installed. This must be considered particularly when it is positioned near components which radiate heat strongly (e.g. valves and power transistors). Furthermore, care must be taken, when bending the wires, that the bending forces do not strain the capacitor housing.

6.8 Installation Position
No restriction.

6.9 Soldering Instructions
Fluxes containing acids must not be used.

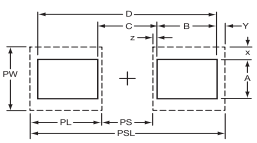
6.9.1 Guidelines for Surface Mount Footprints
Component footprint and reflow pad design for AVX capacitors.

The component footprint is defined as the maximum board area taken up by the terminators. The footprint dimensions are given by A, B, C and D in the diagram, which corresponds to W_1 max., A max., S min. and L max. for the component. The footprint is symmetric about the center lines.

The dimensions x, y and z should be kept to a minimum to reduce rotational tendencies while allowing for visual inspection of the component and its solder fillet.

Dimensions PS (c for F-series) (Pad Separation) and PW (a for F-series) (Pad Width) are calculated using dimensions x and z. Dimension y may vary, depending on whether reflow or wave soldering is to be performed.

For reflow soldering, dimensions PL (b for positive terminal of F-series; b' for negative terminal of F-series) (Pad Length), PW (a) (Pad Width), and PSL (Pad Set Length) have been calculated. For wave soldering the pad width (PWw) is reduced to less than the termination width to minimize the amount of solder pick up while ensuring that a good joint can be produced. In the case of mounting conformal coated capacitors, excentering (Δc) is needed to except anode tab [凸].



NOTE:

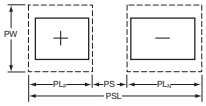
These recommendations (also in compliance with EIA) are guidelines only. With care and control, smaller footprints may be considered for reflow soldering.

Nominal footprint and pad dimensions for each case size are given in the following tables:

PAD DIMENSIONS: millimeters (inches)

Case Size		PSL	PL	PS	PW	PWw
Series	A	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	B	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	2.80 (0.110)	1.60 (0.063)
	C	6.50 (0.256)	2.00 (0.079)	2.50 (0.098)	2.80 (0.110)	1.60 (0.063)
	D	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.00 (0.118)	1.70 (0.067)
	E	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.00 (0.118)	1.70 (0.067)
	F	6.50 (0.256)	2.00 (0.079)	2.50 (0.098)	2.80 (0.110)	1.60 (0.063)
	G	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	H	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	2.80 (0.110)	1.60 (0.063)
SMD 'J' Lead & OxiCap® (excluding F-series)	K	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	L	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	2.80 (0.110)	1.60 (0.063)
	N	2.70 (0.106)	0.95 (0.037)	0.80 (0.031)	1.60 (0.063)	0.80 (0.031)
	P	2.70 (0.106)	0.95 (0.037)	0.80 (0.031)	1.60 (0.063)	0.80 (0.031)
	R	2.70 (0.106)	0.95 (0.037)	0.80 (0.031)	1.60 (0.063)	0.80 (0.031)
	S	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	T	4.00 (0.157)	1.40 (0.055)	1.20 (0.047)	2.80 (0.110)	1.60 (0.063)
	U	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.70 (0.145)	1.80 (0.071)
	V	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.70 (0.145)	1.80 (0.071)
	W	6.50 (0.256)	2.00 (0.079)	2.50 (0.098)	2.80 (0.110)	1.60 (0.063)
	X	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.00 (0.118)	1.70 (0.067)
	Y	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.00 (0.118)	1.70 (0.067)
	Z	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.70 (0.145)	1.80 (0.071)
	5	8.00 (0.315)	2.00 (0.079)	4.00 (0.157)	3.00 (0.118)	1.70 (0.067)
	A	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	B	4.70 (0.185)	1.70 (0.067)	1.30 (0.051)	3.00 (0.118)	1.50 (0.059)
	C	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	D	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	E	0.90 (0.035)	0.30 (0.012)	0.30 (0.012)	0.30 (0.012)	N/A
	H	3.20 (0.126)	1.30 (0.051)	0.60 (0.024)	1.50 (0.059)	0.075 (0.003)
	I	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	J	2.80 (0.110)	1.10 (0.043)	0.60 (0.024)	1.00 (0.039)	0.50 (0.019)
TACmicro-chip® Series	K	2.20 (0.087)	0.90 (0.035)	0.40 (0.016)	0.70 (0.028)	0.35 (0.014)
	L	2.80 (0.110)	1.10 (0.043)	0.60 (0.024)	1.00 (0.039)	0.50 (0.019)
	M	3.20 (0.126)	1.30 (0.051)	0.60 (0.024)	1.00 (0.039)	0.50 (0.019)
	Q	3.20 (0.126)	1.30 (0.051)	0.60 (0.024)	1.50 (0.059)	0.075 (0.003)
	R	3.20 (0.126)	1.30 (0.051)	0.60 (0.024)	1.50 (0.059)	0.075 (0.003)
	S	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	T	4.70 (0.185)	1.70 (0.067)	1.30 (0.051)	3.00 (0.118)	1.50 (0.059)
	U	3.20 (0.126)	1.30 (0.051)	0.60 (0.024)	1.50 (0.059)	0.075 (0.003)
	V	4.40 (0.173)	1.60 (0.063)	1.20 (0.047)	1.80 (0.071)	0.90 (0.035)
	Z	2.80 (0.110)	1.10 (0.043)	0.60 (0.024)	0.70 (0.028)	0.35 (0.014)

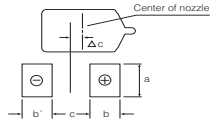
Note: SMD 'J' Lead = TAJ, TMJ, TPS, TPM, TRJ, TRM, THJ, TLJ, TCJ, TCM, TCQ



PAD DIMENSIONS: millimeters (inches)

Case Size		PSL	PL_P	PS	PL_N	PW+	PW-
Series	M	2.50 (0.098)	1.05 (0.041)	0.40 (0.016)	1.05 (0.041)	1.00 (0.039)	1.00 (0.039)
	N	2.50 (0.098)	1.05 (0.041)	0.40 (0.016)	1.05 (0.041)	1.00 (0.039)	1.00 (0.039)
	O	3.60 (0.142)	1.35 (0.053)	0.90 (0.035)	1.35 (0.053)	1.30 (0.051)	1.30 (0.051)
	K	3.60 (0.142)	1.35 (0.053)	0.90 (0.035)	1.35 (0.053)	1.30 (0.051)	1.30 (0.051)
TLN, TCN & J-CAP™ Undertab	S	3.60 (0.142)	1.35 (0.053)	0.90 (0.035)	1.35 (0.053)	1.30 (0.051)	1.30 (0.051)
	L	3.90 (0.154)	1.35 (0.053)	1.00 (0.039)	1.55 (0.061)	2.50 (0.098)	2.10 (0.083)
	T	3.90 (0.154)	1.35 (0.053)	1.00 (0.039)	1.55 (0.061)	2.50 (0.098)	2.10 (0.083)
	H	3.90 (0.154)	1.35 (0.053)	1.00 (0.039)	1.55 (0.061)	2.50 (0.098)	2.10 (0.083)
	X	7.70 (0.303)	2.20 (0.087)	2.10 (0.083)	3.40 (0.134)	3.25 (0.128)	3.25 (0.128)
	3	7.70 (0.303)	2.20 (0.087)	2.10 (0.083)	3.40 (0.134)	4.75 (0.187)	4.75 (0.187)
	4	7.70 (0.303)	2.20 (0.087)	2.10 (0.083)	3.40 (0.134)	4.75 (0.187)	4.75 (0.187)
	6	15.20 (0.598)	2.65 (0.104)	9.90 (0.390)	2.65 (0.104)	5.50 (0.217)	5.50 (0.217)

PAD DIMENSIONS F-SERIES: millimeters (inches)

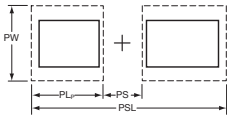


Case Size		a	b	b'	c	Δc*
Series	U	0.35 (0.014)	0.40 (0.016)	0.40 (0.016)	0.40 (0.016)	0.00
	M	0.65 (0.026)	0.70 (0.028)	0.70 (0.028)	0.60 (0.024)	0.00
F38, F39 F91, F92, F93, F97, F9H, F98	S	0.90 (0.035)	0.70 (0.028)	0.70 (0.028)	0.80 (0.032)	0.00
	P	1.00 (0.039)	1.10 (0.043)	1.10 (0.043)	0.40 (0.016)	0.00
	A	1.30 (0.051)	1.40 (0.055)	1.40 (0.055)	1.00 (0.039)	0.00
	B	2.30 (0.091)	1.40 (0.055)	1.40 (0.055)	1.30 (0.051)	0.00
	C	2.30 (0.091)	2.00 (0.079)	2.00 (0.079)	2.70 (0.106)	0.00
	N	2.50 (0.098)	2.00 (0.079)	2.00 (0.079)	4.00 (0.157)	0.00
F95, AUDIO F95 Conformal	R·P	1.40 (0.055)	0.60 (0.024)	0.50 (0.020)	0.70 (0.028)	0.20 (0.008)
	Q·S	1.70 (0.067)	0.70 (0.028)	0.60 (0.024)	1.10 (0.043)	0.20 (0.008)
	A	1.80 (0.071)	0.70 (0.028)	0.60 (0.024)	1.10 (0.043)	0.20 (0.008)
	T	2.60 (0.102)	0.70 (0.028)	0.60 (0.024)	1.20 (0.047)	0.20 (0.008)
	B	2.60 (0.102)	0.80 (0.032)	0.70 (0.028)	1.10 (0.043)	0.20 (0.008)
F72 Conformal	R·M	5.80 (0.228)	1.20 (0.047)	1.20 (0.047)	3.90 (0.154)	0.50 (0.020)
F75 Conformal	U·C	3.00 (0.118)	1.20 (0.047)	1.20 (0.047)	3.30 (0.130)	0.50 (0.020)
	D	4.10 (0.161)	1.20 (0.047)	1.20 (0.047)	3.90 (0.154)	0.50 (0.020)
	R·M	5.80 (0.228)	1.20 (0.047)	1.20 (0.047)	3.90 (0.154)	0.50 (0.020)

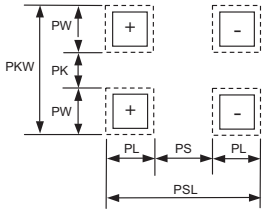
*In the case of mounting conformal coated capacitors, excentering (Δc) is needed to except anode tab [凸].

PAD DIMENSIONS SMD HERMETIC:

millimeters (inches)



Case Size SERIES		PSL	PL	PS	PW	PW_W
TCH & THH J-lead only	9	13.20 (0.520)	2.40 (0.094)	8.40 (0.331)	11.80 (0.465)	N/A
THH J-lead only	I	13.00 (0.512)	3.80 (0.150)	5.40 (0.213)	5.30 (0.210)	N/A
THH Undertab only	I	10.60 (0.417)	3.00 (0.118)	4.60 (0.181)	4.00 (0.157)	N/A



Case Size SERIES		PSL	PL	PS	PKW	PW	PK
TCH & THH Undertab only	9	11.00(0.433)	1.70(0.067)	7.60(0.300)	10.60(0.417)	3.00(0.118)	4.60(0.181)

6.10 PCB Cleaning

Ta chip capacitors are compatible with most PCB board cleaning systems.

If aqueous cleaning is performed, parts must be allowed to dry prior to test. In the event ultrasonics are used power levels should be less than 10 watts per/litre, and care must be taken to avoid vibrational nodes in the cleaning bath.

SECTION 7: EPOXY FLAMMABILITY

EPOXY	UL RATING	OXYGEN INDEX
TAJ/TMJ/TPS/TPM/TRJ/TRM/THJ TLJ/TLN/TCJ/TCM/TCN/J-CAP™ TCQ/NLJ/NOJ/NOS/NOM	UL94 V-0	35%

SECTION 8: QUALIFICATION APPROVAL STATUS

DESCRIPTION	STYLE	SPECIFICATION
Surface mount capacitors	TAJ	CECC 30801 - 005 Issue 2 CECC 30801 - 011 Issue 1