

TECHNICAL PAPER

Voltage Derating Rules for Solid Tantalum and Niobium Capacitors

Tomáš Zedníček

*AVX Czech Republic s.r.o., Dvorakova 328,
563 01 Lanskrout, Czech Republic*

John Gill

*AVX Limited
Long Road, Paignton*

Abstract:

For many years, whenever people have asked tantalum capacitor manufacturers for general recommendations on using their product, the consensus was “a minimum of 50% voltage derating should be applied”. This rule of thumb has since become the most prevalent design guideline for tantalum technology. This paper revisits this statement and explains, given an understanding of the application, why this is not necessarily the case. With the recent introduction of niobium and niobium oxide capacitor technologies, the derating discussion has been extended to these capacitor families also.

Introduction

Conventional tantalum capacitors utilize solid manganese dioxide (MnO_2) as the counter electrode and exhibit excellent steady state reliability thanks to its inherent self-healing behavior [1], [2], [3], [4]. A comparison of failure rate over time for tantalum and aluminium electrolytic capacitors is shown in Fig. 1. below:

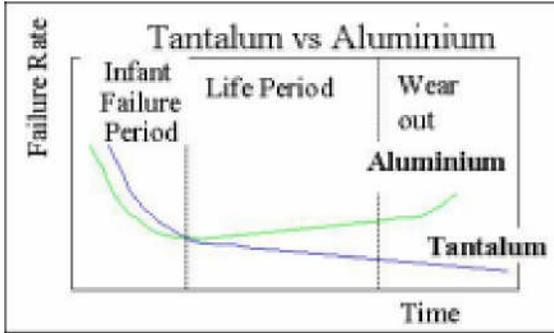


Fig. 1. Failure rate with time on tantalum and aluminium capacitors.

This self-healing process is an important factor in the steady state reliability characteristics of tantalum capacitors, which are referenced as having “no wear out mechanism”. One self-healing reaction is based on thermally inducing oxidization of the conductive MnO_2 counter-electrode and converting into Mn_2O_3 – a higher resistivity form of manganese oxide. The complete reaction is:



If there is an area on the tantalum anode’s dielectric surface that has thinner dielectric than the surrounding area, then the larger proportion of the capacitor’s current (charging, leakage, etc.) will flow through that site (see Figure 2), causing localized heating. As the temperature at the fault site increases, the above reaction [1] takes place converting conductive manganese dioxide (MnO_2), which has a resistivity of between (1 - 10) Ohm/cm², to a less conductive form (Mn_2O_3) having a resistivity between (10⁶ - 10⁷) Ohm/ cm². Thus the conduction site is effectively “plugged” or “capped”, as shown in Figure 3, and the fault current clears.

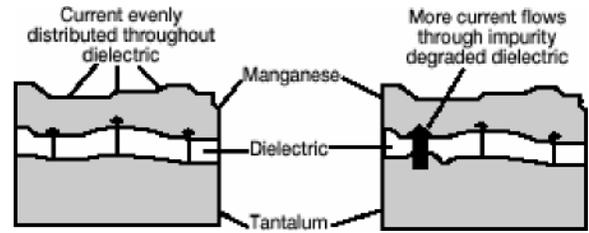


Fig.2. Cross section showing self-healing system

The oxygen produced is absorbed by any lower order tantalum oxides other than tantalum pentoxide (Ta_2O_5) present in the dielectric layer, such as TaO_2 , or any MnO in the counter-electrode layer. See [2] for more details about the self-healing system.

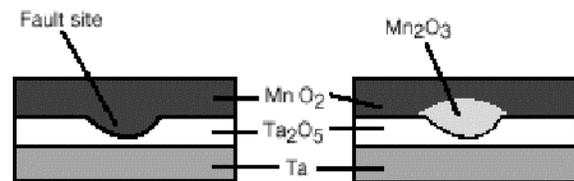


Fig 3. The fault site in dielectric after self-healing process

The self-healing reaction [1] applies to situations where current availability is limited. In the case of high surge currents in low impedance applications, the breakdown of the dielectric can progress faster than the healing mechanisms, and can result in a hard short and complete thermal breakdown. Thus it is of importance to protect tantalum capacitors against any surges that can exceed their design capabilities.

Surge Current

Tantalum capacitor manufacturers have developed hard surge preconditioning tests in order to verify individual capacitor performance under worst-case surge conditions. While there is no defined industry standard for surge screening, individual tantalum capacitor manufacturers have developed their own surge conditioning tests appropriate to their specific designs. The following is a discussion of AVX’s surge screening approach.

AVX have developed a dynamic screening test

which is applied 100% to all product - reference circuit diagram below (Fig. 4)

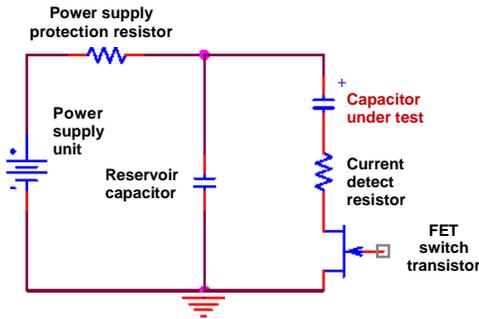


Fig.4. Circuit diagram of surge test circuit

All capacitors are subjected to one or more current surges:

$$I_p = \frac{I \cdot I_x V_R}{R + ESR} \quad [2]$$

where

- I_p = peak current value
- V_R = rated voltage of the capacitor
- R = total series resistance of the test circuit
- ESR = ESR value of the capacitor under test

The total series resistance of test circuit includes all parasitics such as contact resistance, termination and FET resistance etc. The total series resistance is a maximum 1 Ohm for standard product, and a maximum of 0.7 Ohms for Low ESR series (0.45 Ohms on special series). These 100% test values are continually being reduced as new generations of test equipment are developed.

A dynamic monitoring process is used to verify test surge current. The first stage establishes that each capacitor receives the minimum surge current value specified for that particular rating. The test capacitor is rejected if the current surge does not reach this verification level. The second level verifies that the post-test leakage current decays to within a pre-determined level. The test capacitor is rejected if the DCL current exceeds the defined failure level. Fig.5 below shows the surge test cycle.

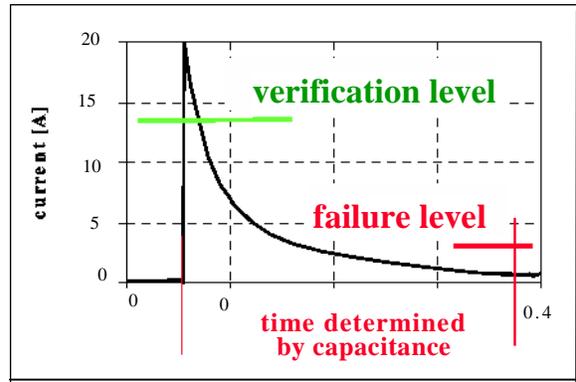


Fig.5. Dynamic monitoring of surge current

Current Through Capacitor

The maximum surge current (transient) through the capacitor in a circuit is defined by two factors:

- a) Power supply output, and
- b) Ohm's law

a) Power supply output

The current developed during power up (charging, transient) through the capacitor depends on the power supply:

$$I = Cx \frac{dV}{dt} \quad [3]$$

where

- C = capacitance of the capacitor
- dV/dt = voltage gradient (how fast the power supply can ramp the voltage)

b) Ohm's law

$$I = \frac{V}{R} \quad [4]$$

where V is the application voltage and R is a total resistance of the circuit.

The actual current through the capacitor is defined by the lower value calculated from equations [3] and [4].

Typical Application

Two typical circuit configurations are shown:

Example 1.

The first case is shown in Fig.6. A simple stabilized power supply circuit consisting of a power source (battery), diode, coil (100nH) and the capacitor:

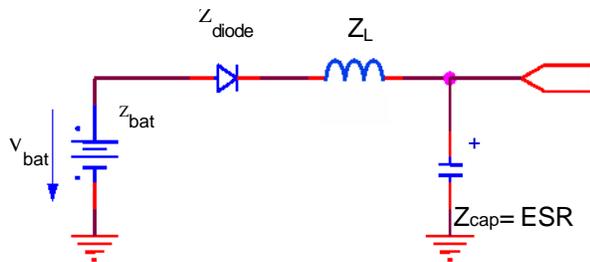


Fig. 6. Typical application Example 1 – simple power source

In the case of an unlimited power supply, the current through the circuit is defined by Ohm's law only; e.g. current from [3] is much higher than [4].

Example of max current calculation:

V_{bat} = 3.2V (2 cell battery)
 Capacitor = 220µF 6.3v low ESR, surge tantalum capacitor. The 100mΩ. 6.3V capacitor is selected by 'rule of thumb' 50% derating rule e.g. 6.3V capacitor is used for the 3.2v o/p.

Typical resistance of circuit components:

Z_{bat} = 60mΩ, Z_{diode} = 70mΩ, Z_{L(100kHz)} = 70mΩ, Z_{cap} = ESR_(100kHz) = 100mΩ

Hence, the max current through the circuit based on [4] is:

$$I = \frac{V}{R} = \frac{3.2}{0.06+0.07+0.07+0.1} = 10.7A \quad [5]$$

The D case 220µF 6.3V 100mΩ is designed and tested for peak current surge in accordance with [2] (R=0.7 for surge robust series):

$$I = \frac{1.1xV_R}{R + ESR} = \frac{1.1x6.3}{0.7+0.1} = 8.7A \quad [6]$$

The application surge current available per equation [5] is higher than the peak current [6] that is used for the capacitor preconditioning.

The 50% derating rule in this case is not sufficient to prevent the capacitor against overload. The application requires a higher level of derating (e.g. a 10v rated capacitor).

Example 2.

Consider the circuit below:

In this case the tantalum capacitor (C2) is used on the output of a DC/DC converter – see Fig. 7.

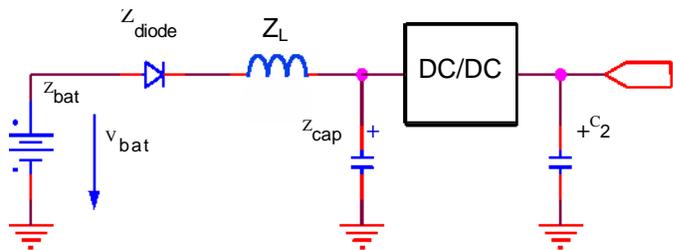


Fig. 7. Typical application Example 2 – DC/DC converter

DC/DC converters control the transient power buck/boost sequences. In such case the maximum current through the capacitor C2 would be ~ 1A maximum. Hence the surge current through capacitor C2 would be considered within the capability of the capacitor.

A tantalum capacitor with derating factor as low as 20% could be used in this application.

Soft-start circuit

One alternative when a tantalum capacitor must be used in low impedance application is to use a "soft start circuit" and thus eliminate the transient surge current load – as happened in Example 1. A typical example of such a soft start circuit diagram is shown in Fig. 8 below:

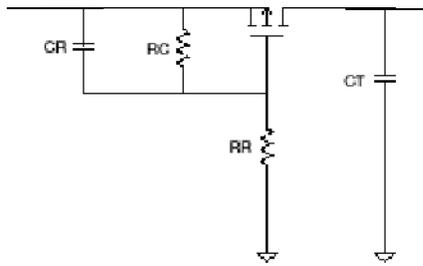


Fig. 8. Simple soft-start circuit diagram

A FET transistor, plus one small capacitor and two resistors can suppress the transient effect. This provides a low cost solution that will yield long term reliable operation of the circuit by reducing transient loading all circuit components – not only the tantalum capacitors. More details including this soft start component calculation are given in ref. [11].

Parameters Sensitive to Derating

There are three main parameters sensitive to the level of derating (ratio between applied voltage and rated voltage of the capacitor): Steady State Failure Rate, Dynamic Failure Rate (resistance to surge current / low external resistance) and DCL at application voltage.

1] Steady State Failure Rate

The useful life reliability of the tantalum capacitors in steady state is affected by three factors. The equation from which the failure rate can be calculated is:

$$F = F_U \times F_T \times F_R \times F_B \quad [7]$$

where

F_U is a correction factor due to operating voltage/voltage derating

F_T is a correction factor due to operating temperature

F_R is a correction factor due to circuit series resistance

F_B is the basic rate level

Operating voltage/voltage derating – F_U factor

The operating reliability will be improved if a capacitor a higher voltage rating than the maximum line voltage is used. For more details see ref. [5].

Example of effect on derating to the failure rate:
Operating conditions: 85°C, 5V, 0.1 Ohm/V series resistance.

Case 1 – 6.3V tantalum capacitor

Reliability factors based on ref. [5]:

$F_U = 0.12$, $F_T = 1$, $F_R = 1$, $F_B = 1\%/1000hrs$
the failure rate from eq. [7]:

$$F = F_U \times F_T \times F_R \times F_B = 0.12 \times 1 \times 1 \times 1 = 0.12\%/1000hrs$$

per MTBF definition:

$$MTBF = \frac{10^5}{F} = \frac{10^5}{0.12} = 95 \text{ years}$$

Case 2 – 10V tantalum capacitor

Reliability factors based on ref. [5]:

$F_U = 0.007$, $F_T = 1$, $F_R = 1$, $F_B = 1\%/1000hrs$
the failure rate from eq. [7]:

$$F = F_U \times F_T \times F_R \times F_B = 0.007 \times 1 \times 1 \times 1 = 0.007\%/1000hrs$$

$$MTBF = \frac{10^5}{F} = \frac{10^5}{0.007} = 1,631 \text{ years}$$

In summary, MTBF will improve by factor of 17 in this case when 10V capacitor was used instead of 6.3V on 5V rail.

2] Dynamic Failure Rate (Surge Current)

Protection against uneven current surges in low impedance circuits is the most important factor to consider an appropriate derating factor of tantalum capacitor. The worst case of current surge in the application should not exceed the design and screened current of the capacitor per equation [2] see example in paragraph above.

3] DCL - leakage current in the application

The leakage current drops rapidly below the value corresponding to the rated voltage V_R when reduced voltages are applied.

Example: typical DCL of 10V capacitor used at different operating voltage – see table Fig 8 below.

Operating Voltage [V]	Typical DCL [μ A]
10V rail	10 μ A
5V rail	2.5 μ A
3.3V rail	1.5 μ A

Fig.8. Typical effect of operating voltage to DCL on 10V capacitor

DCL value can typically drop to one range lower value if 50% derating is used. More details – see ref. [6].

Niobium based capacitors

New types of capacitors based on niobium powders have been introduced recently to the market. The technology process is very similar to the tantalum capacitor, however niobium replaces the tantalum anode material. Unlike tantalum, which can only be used in metal form, there are two types of niobium based material that can be used for the anode – Nb niobium metal and NbO niobium oxide. Based on the similarity in features all the derating principles mentioned already in this paper are valid also for niobium metal capacitors. However, for capacitors made from niobium oxide, the failure-rate has less dependence on applied voltage and have different derating requirements For more details on Niobium Capacitors see refs. [7], [8], [9], [10].

Derating of Niobium Oxide Capacitors

Niobium Oxide has two orders higher ignition energy and twice the specific heat of both tantalum and niobium metals - see Figures 9 and 10:

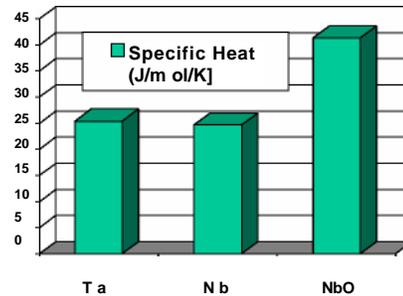
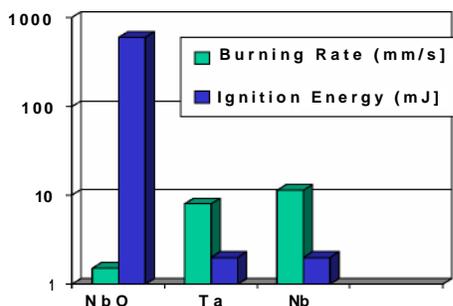


Figure 9,10. Comparison of Ignition Rate, Ignition Energy and Specific Heat for NbO, Ta and Nb metal powders

Note: Specific heat [J/mol/K] is the energy needed to heat a unit volume (1mole) by 1Kelvin.

Niobium suboxides may be responsible for a unique high resistance dielectric breakdown failure mode of these capacitors. When the main dielectric (Nb_2O_5) is broken either electrically by overvoltage or thermo-mechanically (by overheating during reflow process for example) the NbO capacitors will not fail with short circuit as any other capacitor made by other technology, but it will change to high resistance typically about 34kOhm. The capacitors maintain its electrical performance and the end device may be still operational. Hence it can be stated that a failed NbO capacitor will not burn up to category voltage. See more details at [12], [7], [8]. Coupled with the lower electrical stress within the dielectric (Nb_2O_5 dielectric grows thicker per applied volt than Ta_2O_5 and so operates at lower field strength for a given voltage rating), this also enables a higher ripple current load and **reduced voltage derating** requirements in low impedance circuits.

Hence a minimum derating of 20% is sufficient in all applications; so, for example, a 4V capacitor can be safely used on a 3.3v power rail and a 6.3v rated capacitor on a 5.5v rail.

Derating Software

A software tool has been now developed to simplify the calculations related to derating guidelines. This can help the circuit designer to optimize circuit designs within the defined tantalum and niobium capacitor specifications.

Input fields:

1. Applied (operational) Voltage
2. Circuit Resistance (excluding capacitor's ESR)
3. Optional – di/dt ; dV/dt of the power source - series and part details

The software calculates current surge from the given entry parameters e.g. equations [3] and [4] are calculated together with [2] from the build in or external capacitor database.



Fig 11. Input screen of the derating software

The software then displays those ratings available that meet design requirements: the designed and screened current [2] is greater than or equal to the maximum current in the application (lower value from [3] and [4]).

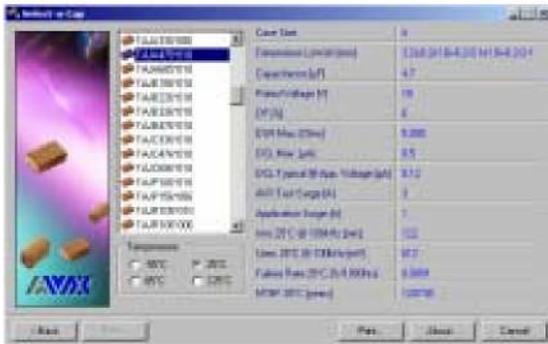


Fig 12. Input screen of the derating software

Once the software creates list of the “safe” available capacitors it is possible to calculate more application data for each of them. The output fields displayed when a specific part is selected are:

1. Specifications (Cap, ESR, DCL, DF, Case & Dimensions)

2. DCL at application voltage.
3. Continuous maximum ripple current and voltage
4. Failure rate, FIT and MTBF
5. Temperature effect in steps $-55, 25, 85, 125^{\circ}\text{C}$ for parameters 2,3 and 4 above

The software based on the input application conditions selects the correct part(s) considered to be “safe” for the design. The additional data given will also help to optimise selection of capacitor for other application requirements.

Conclusion

- Voltage derating is necessary for tantalum and niobium capacitors to prevent failure due to excess current availability.
- Tantalum capacitors can be safely used at 80% of their rated voltage, but the MTBF will be lower and leakage current higher.
- If a tantalum must be used across a low impedance source, consider incorporating a PFET integrator to reduce risk of failure.
- A 20% derating is sufficient for OxiCap™ NbO capacitor in most applications.
- Select-a-Cap software is available to help identify the correct part number including typical parameters in a given application.

REFERENCES

1. P.Vasina & col., “Failure modes of tantalum capacitors made by different technologies”, CARTS USA 2001 Florida
2. J.Gill, “Surge in solid tantalum capacitors”, AVX technical paper, www.avxcorp.com
3. J.D.Prymak, “Replacing MnO_2 with conductive polymer in tantalum capacitors,” Kemet Corp. CARTS EUROPE 1999 Lisbon Portugal, pp. 169-173
4. N. Klein, “Electrical breakdown in thin dielectric films,” J. Electrochem. Soc., Solid State Science, 116, 963 (1969)
5. AVX Surface Mount Tantalum Catalogue, Pg 45, www.avxcorp.com

6. R.W.Franklin, "An Exploration of Leakage Current", AVX technical paper, www.avxcorp.com
7. T.Zednicek & col., "Niobium Oxide Technology Roadmap", CARTS EUROPE 2002 Nice, France, proceeding
8. T.Zednicek & col., "Tantalum and Niobium Technology Overview", CARTS EUROPE 2002 Nice, France, proceeding
9. Y.Pozdeev-Freeman & col., "Niobium Based Solid Electrolytic Capacitors", CARTS USA 2002, New Orleans, Louisiana, USA, proceeding
10. H.Zillgen & col., "New Niobium Capacitors with Stable Electrical Parameters", CARTS USA 2002, New Orleans, Louisiana, USA, proceeding
11. D.Mattingly, "Increasing Reliability of SMD Tantalum Capacitors in Low Impedance Capacitors", AVX technical paper, www.avxcorp.com
12. J.Sikula & col., "Conductivity Mechanism and Breakdown Characteristics of Niobium Oxide Capacitors" CARTS Europe 2003, Stuttgart, Proceeding



NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250

NOTICE: Specifications are subject to change without notice. Contact your nearest AVX Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.

