TECHNICAL PAPER

Selecting Back-Up Capacitors for Modern Solid State Drives

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Abstract:
High speed cache memory greatly improves SSD performance. Providing a power backup for DRAM buffer memory assures no data loss on power switch off or failure, and also improves speed and reaction time after power on.

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Several SSD power supply backup options are available:
1) Secondary Battery: a simple solution, but lifetime is a relatively short - about 500 cycles - and expensive, especially when integrated into the IC package.
2) Supercapacitor: Although these devices can offer a high capacitance and store enough energy for DRAM buffer flushing into the Flash memory, they have a relatively-high ESR, which effectively limits energy flow. Also, most supercapacitor technologies have a narrow working temperature range - c70degC only - which prohibits standard automated reflow soldering leading to hand soldered, increasing assembly time and costs.
3) Tantalum capacitors: When stacked in parallel, these devices provide enough capacitance to deliver the energy needed for data flushing. They are also compatible with standard, automated lead-free reflow soldering processes and are very reliable.

Designing a power supply for an SSD

The backup supply for an SSD must provide sufficient power to transfer essential data from the fast DRAM buffer memory into non-volatile Flash memory should the power fail. When a capacitor is being used as an energy reservoir, its voltage drops as its energy drains. Therefore, the first stage DC/DC converter in an SSD power system should be a Buck-Boost type, which is able to step up the voltage at the end of capacitor discharge period.

Consider a modern SSD with 5V supply voltage, reduced power consumption, P, (in data write mode) of 0.22W and typical DRAM buffer memory size of 64MB. If the speed of data write into Flash memory is 140MB/s, the minimum time for full buffer flushing from DRAM to Flash (t_f, = memory size/write speed) is 457ms. Obviously the backup time t_b that must be provided by the reservoir capacitor to enable full buffer flushing into the SSD Flash memory needs to be bigger than flush time.

It is useful to simulate the capacitor discharge process based on constant power consumption and energy flowing to the input of the Buck-Boost converter. Assume disconnection from external power supply in zero seconds and capacitor discharge to be U_c = 0V (ideal converter or ‘energy harvester’).

The basic capacitor formula for current is:

$$I = C*dU/dt$$

where current I is given by the constant current consumption, I = P/U, which will increase as the voltage of capacitor drops.

The ESR of the capacitor may also affect backup time, due to thermal energy loss. The current draining from capacitor causes an additional voltage drop, therefore the input DC/DC converter increases the actual value of the current to cover full power demand.

$$U_{cext} = U_{cint} – ESR*I.$$

In this example, the value of backup capacitor capacitance, C, has been estimated as 9mF. In order to save PCB space, new high capacitance/low profile PulseCap capacitors from AVX were selected.

Possible solution at 85degC

In order to achieve the required operating voltage of 5V at 85degC and 9mF capacitance, a stack of nine TLN4108M010R0100 1mF PulseCap capacitors can be connected in parallel. These devices have an ESR_{max} of 100mΩ at 100kHz and a DCL_{max} of 100µA at 25degC. Individual capacitors have a footprint of 7.3x6.1 mm and a height of 2mm. They use an 'Undertab' construction with solder pads on the under side only. Therefore a 'block' of nine devices measures 21.9 x 18.3 x 2 mm.

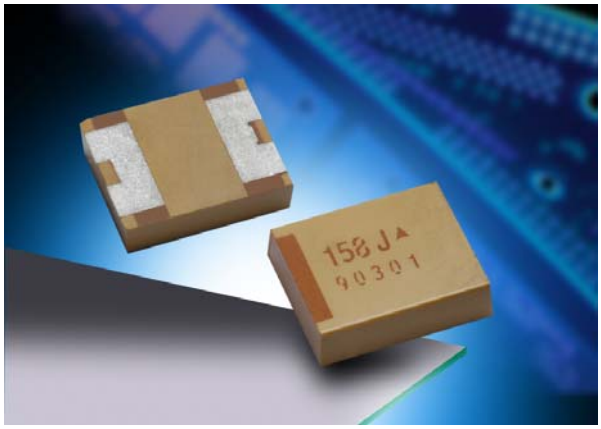

Fig. 1 – Pulsecap TLN4 SMD tantalum capacitor using Undertab construction

A first simulation of the discharge energy reservoir shows a discharging time = backup time, t_{b1}, = 514ms.
The maximum ESR of the stack of capacitors is given by ESR_{max} multiplied by 4.5 (a factor for DC ESR) and divided by 9 for parallel combination.

$$ESR_{smax} = 100*4.5/9 = 50mΩ$$

This is a relatively low figure, so thermal energy losses are negligible, only reducing backup time to 506ms, (By contrast, supercapacitors exhibit higher ESR than solid tantalum capacitors, when comparing similar nominal capacitance parts. For example a BZ05 supercapacitor has an ESR_{max} of 600mΩ at 1kHz, which is nearly the

same for DC conditions.

The leakage current, DCL, of reservoir capacitors causes self-discharging and behaves as an additional load so its effect must also be considered. TLN4108M010 capacitors have a leakage current, DCL_{max25} of 100µA (at 25degC, rated voltage, steady state (after 5 minutes)). The worst case (highest) value of DCL is at the highest operating temperature (85degC). A factor of 7.75 can be used for recalculating DCL at 85degC, according to: $DCL_{max85} = 7.75*DCL_{max25}$, and allowing for the parallel connection of parts, $DCL_{max85s} = 9*DCL_{max85}$

The application voltage in this backup application is 50% of rated value or lower, depending on the phase of discharge. Hence the leakage current is reduced with respect to the actual derating factor. (Leakage current estimation is discussed in an article entitled: 'Low Leakage Current Aspect of Designing with Tantalum and NbO Capacitors', available at http://www.avx.com.)

When the maximum DCL for worst-case operating conditions is considered (DCL_{85s1} = 6975µA), the backup time for the TLN4 SMD tantalum capacitors must be reduced from 514ms to 504ms - quite a minor difference and likely to be even smaller if we accept that the real leakage currents are typically far below their maximum datasheet limits.

However, if were to consider using tantalum polymer capacitors rather than PulseCap TLN4 tantalums, there is a considerable change. Ta-Poly technology capacitors have a much high leakage current (10x DCL) than pure tantalum devices, so DCL_{85} is 69750µA. Such high DCL level significantly affects backup time, shortening back up time to 430ms and renderng them unsitable for this application.

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