



TECHNICAL INFORMATION

INTERCONNECT SCHEMES FOR LOW INDUCTANCE CERAMIC CAPACITORS

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Abstract:

As digital electronic systems continue to operate at higher and higher frequencies, the use of low inductance decoupling capacitors continues to increase. The parasitic inductance of the devices themselves is important, but the method used to connect the components to the system, such as printed circuit boards (PCB), is also a considerable factor. Adding inductance in the connection scheme can eliminate some of the effectiveness of the use of these low inductance elements. This paper will examine some of the different schemes utilized at the board level to minimize the loop inductance of the decoupling capacitors.

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Introduction

The only method shown to date that lowers the inductance of a ceramic capacitor is to alter the form factor. By changing the length and width of the current paths through the units. One of the first devices available in the market place are the so-called 'reverse geometry' capacitors. These components are often referred to from the industry standard case designators as 0612, 0508 and 0306 and Figure 1 shows the difference between a more common capacitor, such as a 1206. Terminating the devices in the longer of the two directions is an effective method for lowering the parasitic



Fig. 1 - 1206 vs. 0612

inductance and it basically cuts the value in half.

Another method that has shown itself to be effective in lowering the inductance value of the capacitors is multiple terminations. One device on the market today is the InterDigitated Capacitor (IDC). This is an eight terminal component that contains one capacitor, as shown in Figure 2.

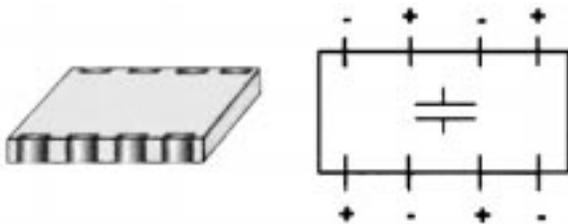


Fig. 2 - IDC configuration

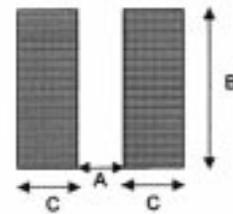
This non-polar device is connected to the power/ground planes by alternating each termination to the individual planes. These devices are available in both 0612 and 0508 versions. Table I lists the measured inductance values for each of the different case sizes.

Case Size	Inductance (pH)
0612	550
0508	500
0306	400
0612 IDC	175
0508 IDC	110

Table I

Reverse Geometry

The first step to attaching components to a PCB are the pads. The recommended pad layouts for all the reverse geometry case sizes is shown in Figure 3.



Case	A	B	C
0612	.030"	.120"	.035"
0508	.020"	.080"	.030"
0306	.015"	.060"	.020"

Fig. 3 - Pad layouts for reverse geometry chips

Once the pads are determined, the next step is to connect the pads to the internal planes with vias. Due to the increase in length of the pads, it is recommended that one use multiple vias to each pad to reduce the total inductance seen by the decoupling capacitors. Different board level manufacturers require different minimums for via pitch due to routine reasons, with most being around 0.050". If this indeed is the case, then the 0612 should have 3 vias per pad and the 0508 and 0306 packages two, as shown in Figure 4.

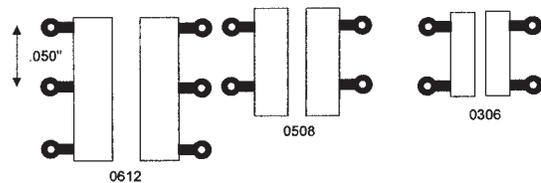


Fig. 4 - Different via schemes for reverse geometry

Obviously, if one can do less pitch between vias then the more vias that can be added will improve the electrical performance. It should also be noted that the trace

between the via and the pad be kept as short as manufacturing limitations will allow.

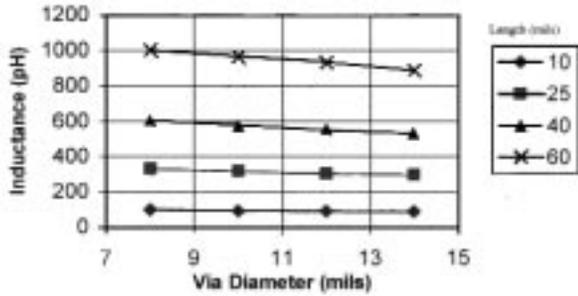


Fig. 4 - Different via schemes for reverse geometry

Via Inductance

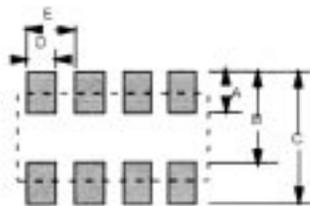
The vias are a natural inductor in the shape of a hollow or solid tube. The value of inductance is directly proportional to the length and diameter of the tube. Figure 5 shows the inductance of a via for a variety of lengths and diameters. Obviously the best method for keeping this number down is to keep the power and ground planes as close to the top/bottom of the PCB as possible. While this is not always prudent, it is very common to find ground planes on top and bottom, with the power plane in the middle of the PCB. As shown in Figure 5, running a decoupling capacitor via all the way through a 60 mil circuit board can add ~1nH of inductance.

Via in Pad

Another significant method for reducing the inductive loop created in connecting a decoupling capacitor to a board is by placing the vias in the pads. This eliminates the inductance caused by the traces connecting the via to the pad. While some manufacturers will not allow this practice, more and more are going to this type of technique to help improve the overall performance of the system.

IDC Interconnect

The IDC presents a different challenge to connect the terminals to the power/ground planes. The most obvious being the fact that board designer has no choice but to go to the component with 8 vias. The pad layout for the IDC is shown in Figure 5.



Case	A	B	C	D	E
0612	.035	.065	.100	.018	.030
0508	.025	.050	.075	.011	.020

Fig. 5 - Pad layout for the IDC

The first point should be that the pitch for these devices is much smaller than your average capacitor, with the 0612 at 30mils and the 0508 at 20mils. The options for a 50mil minimum pitch board are limited. One scheme is shown in Figure 6. Keep in mind that although a 0508 is shown, it would not be the best possible connection scheme. A much finer pitch would have to be used to get the best possible performance, but due to the fact that eight vias are going to this device it's operation would still be superior to two terminal devices. This scheme violates the minimum pitch rule in one direction, keeps it for the other. A tradeoff that has to be made to realize the benefit of the IDC.

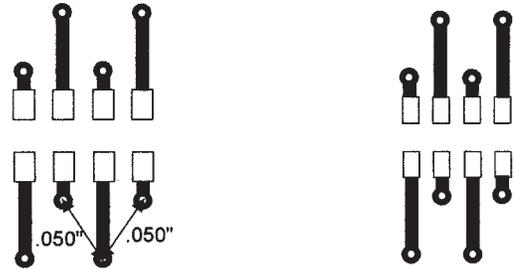


Fig. 6 - IDC connection scheme for 50mil minimum pitch

If the manufacturing process allows .030" minimum pitch then the 0612 IDC is relatively simple, as the vias come straight off the pads. The 0508 IDC would have to be connected in a fashion similar to Figure 6.

Progresses in board manufacturing, such as microvias and via in pads, lead to interesting attachment methods for IDCs. A variety of ideas that have been demonstrated are shown in Figure 7.

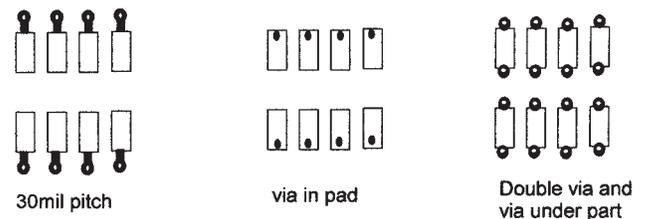


Fig. 7 - Variety of IDC attachment schemes

Conclusions

This paper presents an overlook at the attachment of low inductance decoupling capacitors. The basic rule being that the more vias to a given part, the better the loop inductance caused by attachment to the power/ground planes. All the examples shown here are limited by the technology used to manufacture and load PCBs. Cost considerations for a given technology would have to be weighed against the need to truly attach these devices efficiently.

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