TECHNICAL PAPER

Parameters Important For Surface Mount Applications Of Multilayer Ceramic Capacitors

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Abstract

With increasing use of multilayer ceramic capacitors (MLCs) in surface mount technology (SMT), the understanding of the mechanical properties and thermal stress resistance parameters of MLCs is essential for zero defect soldering and sub ppm failure rates. In this paper, various aspects of SMT including zero defect design, placement considerations, soldering techniques, thermal stress resistance parameters, and post solder handling are reviewed. Special emphasis is given to parameters responsible for thermal shock behavior of MLCs with review of the effect of overall component thickness, temperature gradients, and terminations of MLCs.

PARAMETERS IMPORTANT FOR SURFACE MOUNT APPLICATIONS OF MULTILAYER CERAMIC CAPACITORS

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Introduction

A detailed review of various aspects of surface mount manufacturing has been undertaken to understand various sources of defects which may arise in multilayer ceramic capacitors (MLCs) after assembly. In line process modifications, marginal components, and rework are no longer acceptable for obtaining sub-ppm failure rates of surface mount assemblies. It is essential to understand the design considerations and possible sources of defects in these assemblies, and it is mandatory that the zero defect soldering designs be used and be manufacturable. The next aspect of this subject is the understanding of placement of MLCs on boards and various considerations thereof to have zero defect placement before any reflow is carried out. Soldering techniques themselves are then considered to understand the needs of the mechanical and thermal properties required from MLCs. Post solder handling is reviewed as this may cause defects and result in early failures.

Various aspects of the thermal stresses of MLCs are reviewed and some experimental results are reported; emphasis is placed on, as an example, a detailed understanding of the termination of MLCs. The complexity of this part of the study clearly shows that various models need modifications to really understand the behavior of MLCs.

Various tests to review the reliability of MLCs on test boards are outlined and failure rates are estimated.

Review of Surface Mount Manufacturing

Zero Defect Design

Surface mount technology (SMT) for assembly of boards primarily uses reflow soldering techniques which include infra-red reflow and vapor phase, and uses wave soldering. In reflow soldering, solder is applied prior to placement of components and wave soldering is an additive process as solder fillet is formed as a result of transfer of solder from a reservoir of molten solder. For reflow soldering techniques, the parameters important for zero defect soldering are:

(i) *Solder Mass:* When the solder reflows, surface tension forces exerted by the molten solder are counteracted by the mass of the device and the moment arm created by the component length and adhesion of molten solder to the opposite end. Too much solder results in drawbridging or a missing solder joint for MLCs, small outline transistors (SOTs), and small integrated circuits (ICs). Inadequate solder results in weak or missing solder joints for passive components or coplanarity problems with ICs. It is therefore recommended that the total equivalent wet laydown of solder paste should be 0.25 - 0.30mm and must take the board solder plating into account.

(ii) *Pad Design:* There is a profusion of recommended pad designs by component manufacturers, government agencies, industry associations, and component users, and comprehensive details are available from The Institute for Interconnecting and Packaging Electronic Circuits with details in IPC-SM-782[13]. It should be noted that this document contains compromises of many industry representatives and may not have an understanding of the impact of yields. Therefore, the best source for pad designs are users or vendors that have reliable, low defect solder joint histories. These designs should be tried and tested for manufacturing followed by thermal cycling and environmental testing.
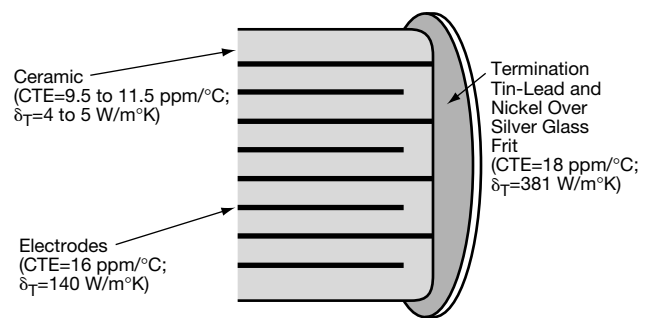

Figure 1. MLC Structure with CTE and δ_T Listed

(iii) *Trace-Pad Interactions:* Details of parameters for reflow soldering and trace-pad interactions are common industry practice[1,13]. Briefly, the designs should limit the numbers of traces entering a pad, the traces entering the pad should be symmetrical, and there should be no vias or through holes in a pad. In addition, the ground planes should be isolated from components with necked down conductors, and via pads should be isolated from the component pads. Examples are shown in Figures 1(a) and (b).
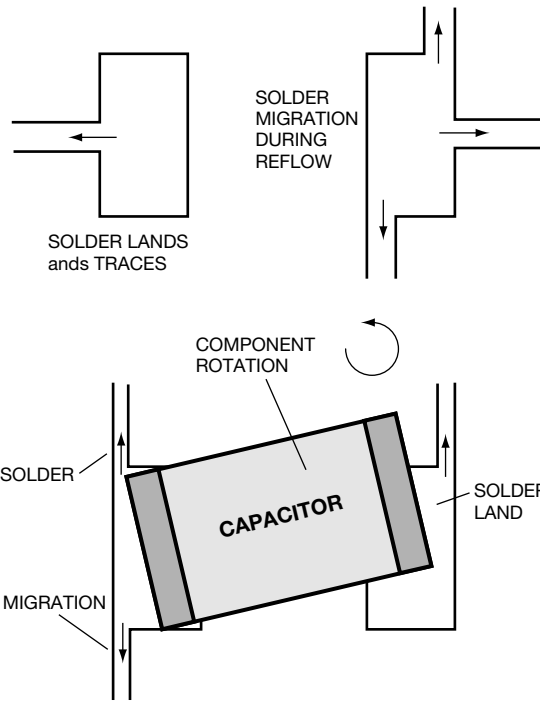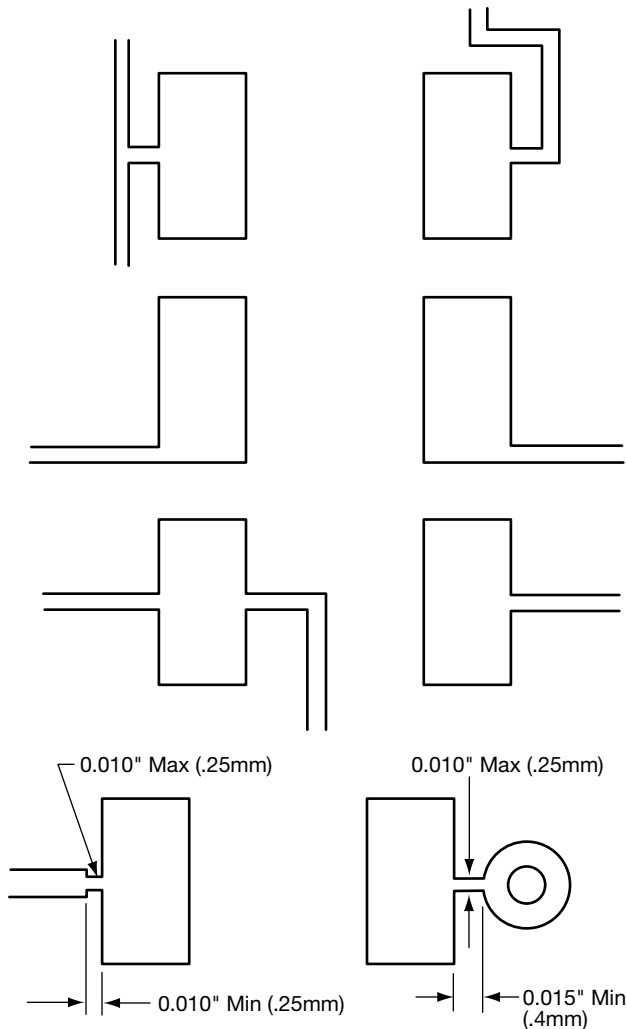
Figure 1(a). Design Techniques to Avoid

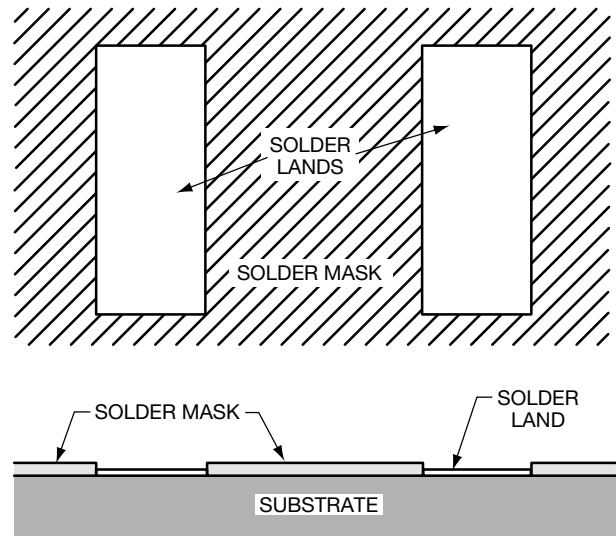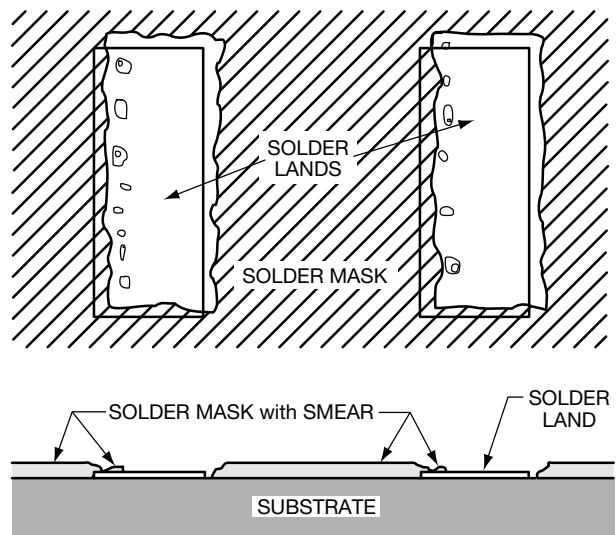Figure 1(b). Design Techniques that Work

Figure 2(a). Ideal Solder Mask

Figure 2(b). Actual Solder Mask

(iv) *Solder Mask Design:* Solder mask artwork should be oversized[1,13] by 10 mils in each dimension to allow for artwork misregistration or slump of wet film to avoid contamination of pad surface; examples are shown in Figures 2(a) and (b). In addition, elimination of solder mask between pads eliminates solder mask thickness problems as shown in Figures 3(a) and (b).

(v) *Component Orientation:* These defects are a result of low mass component termination and differential heating. Each termination should enter the solder zone simultaneously, and low mass transistors and ICs need to enter along the long axis.

For wave soldering, the parameters important for zero defect soldering are:

(i) *Orientation and Placement:* Once again, uniform exposure of component terminations to the solder
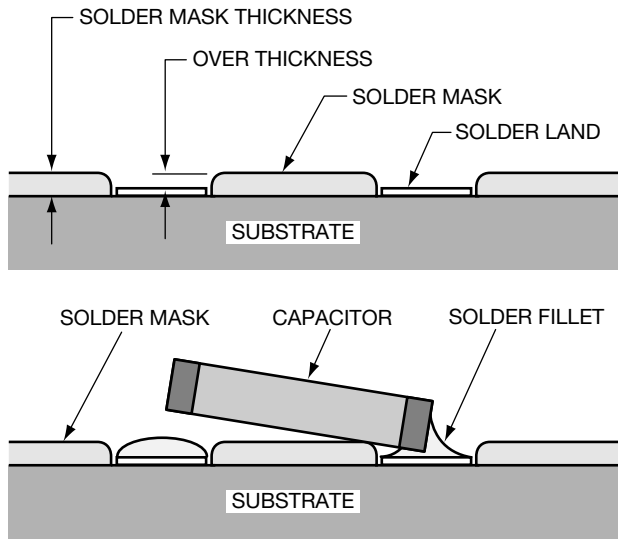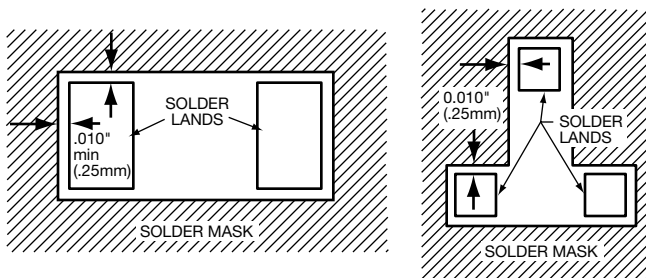
Figure 3(a). Solder Mask Induced Drawbridge

Figure 3(b). Chip and SOT Solder Mask Opening

bath is critical to achieve low defects and reliable solder joints as shown in Figure 4. In addition to orientation, components cannot be upstream of terminations that are to be soldered as starved or missing solder joints will result. In addition, small components cannot be in the shadow of large ones.

(ii) *Pad Designs:* For wave soldering, large solder fillets are easy to inspect but they dramatically reduce solder joint life and make the whole assembly more susceptible to handling damage. It is essential that pad sizes with known high yields be used.
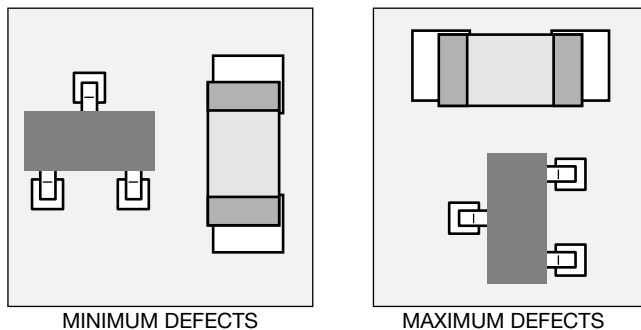
COMPONENT ORIENTATION AND DEFECTS

Figure 4. Component Soldering Orientation

In addition to the above, designs should include considerations for tooling holes, test points, component separation, power/ground planes, and post solder assembly stresses. Details of these are outlined by Maxwell[1].

Pick-and-Place Damage

Defects caused by pick-and-place are erroneously referred to as "thermal shock cracks" and are one of the largest sources of defects in surface mount assembly. This category of defects may result from centering jaws or vacuum pick-up bits and are briefly described below:

(i) *Vacuum Pick-Up Bits:* This defect is visible as a circular or a half-moon shaped crushed area with ragged edges and is caused by excessive z-axis placement force. Another possible manifestation of the excessive placement force is where, for reflow soldering, the terminations are supported by solder paste allowing the unsupported component body to crack in the flexure mode. Pneumatic actuators may be used but component thickness variations, air pressure variations, solder thickness variations, and board warpage should be monitored. In summary, z-axis placement force has to be monitored and controlled for zero placement defects.

(ii) *Centering Jaw Damage:* Even though machine vision is being increasingly used, centering jaws (or mechanical alignment) are used extensively to center and orient the components before placement. Typical pick-and-place machine jaws are 1mm wide and 0.25 - 0.5mm deep, and this results in small contact areas between the jaw and the components resulting in cracked components as shown schematically in Figure 5. In addition, worn out jaws or misorientation of
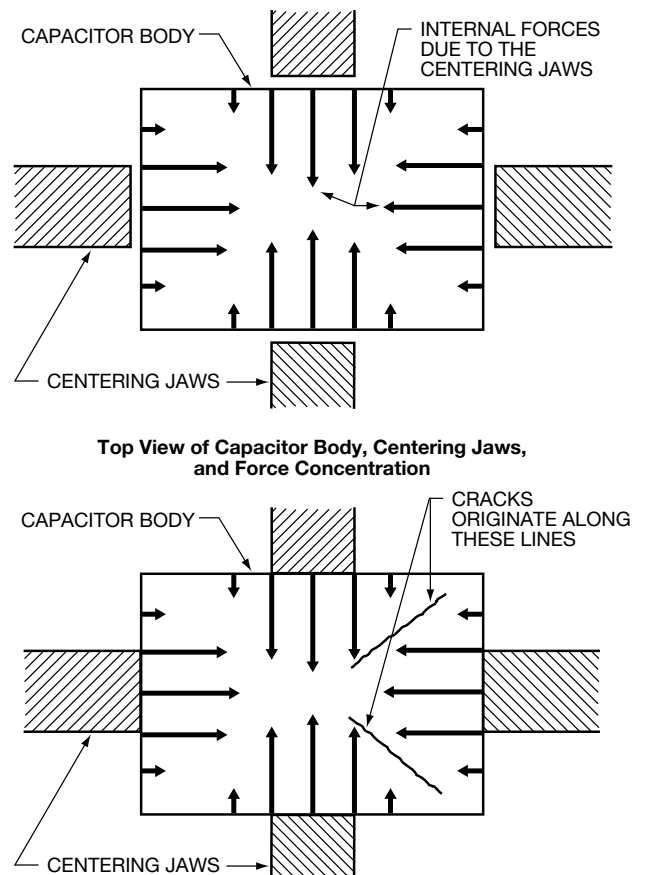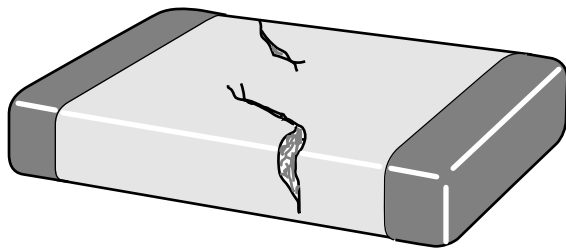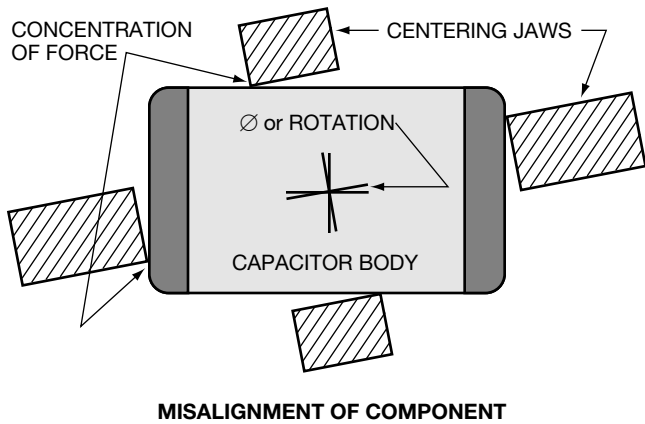

Top View of Capacitor Body, Centering Jaws, and Force Concentration

Figure 5. Top Centering Jaw Damage

CONCENTRATION OF FORCE — CENTERING JAWS

∅ or ROTATION

CAPACITOR BODY

MISALIGNMENT OF COMPONENT

Figure 6. Carrier Tape Misalignment Damage by Centering Jaws

215-219°C

NATURAL COOL DOWN

183°C

45-60 SEC ABOVE SOLDER MELTING POINT

100°C

ALLOWS UNIFORM BOARD HEATING

PREHEAT ZONE ACTIVATES SOLDER FLUX

Figure 7. IR Reflow Solder Profile

212°C

>50°C/SEC

45-60 SEC ABOVE SOLDER MELTING POINT

183°C

NATURAL COOL DOWN

PREHEAT ZONE

Figure 8. Vapor Phase Reflow Solder Profile

components result in near-point contacts and high concentration of stresses causing chipouts at the impact points and this is schematically shown in Figure 6.

Soldering Techniques

As described earlier, infra-red (and hot-plate) and vapor phase reflow techniques involve screening of solder paste, placement of components, and reflow of solder whereas wave solder technique involves gluing the components on a substrate followed by sending this assembly over a solder bath. Details of process profiling are covered in the literature[3,14] and are summarized below:

(i) *Infrared (IR) and Hot Plate Reflow:* For IR reflow, heat conducts from the substrate to component land patterns where the screened paste reflows to form the solder joints. For the formation of a good solder fillet formation, the main parameters are complete solder paste melting, minimum solder migration away from the fillet, and minimum component temperature exposure. The maximum rate of use or cool down of temperature in an IR reflow profile should be 4°C/sec. and a peak temperature of 215-219°C with 45-60 seconds above the melting point for Sn/Pb eutectic solders. Before the maximum temperature is reached, the boards are allowed to soak in the preheat zone at 100° and at 150°C to activate the flux and to allow uniform heating of the board respectively. A recommended profile is shown in Figure 7.

(ii) *Vapor Phase Reflow (VPR) Soldering:* VPR uses surface heating from the latent heat of vaporization of the condensing vapor to reflow the solder paste. Preheat is suggested to avoid rapid rates of temperature in excess of 50°C/sec. to activate solder flux and to drive off the solvent volatiles. Natural cool down is
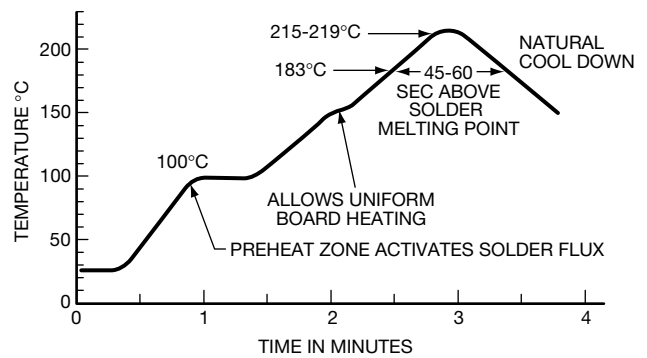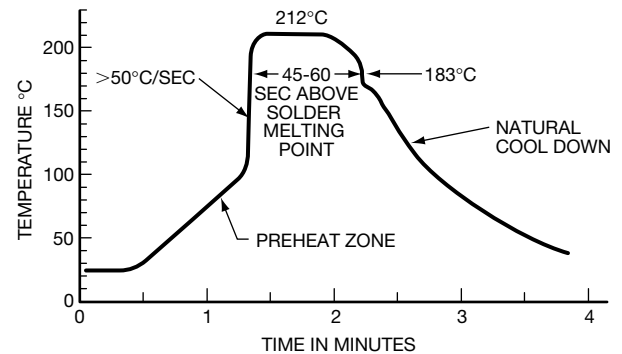
also used to eliminate rapid changes in temperature. A preferred reflow profile is shown in Figure 8.

(iii) *Wave Soldering:* This process uses infrared preheat and liquid solder pots resulting in very rapid rates of heat transfer from preheat to the actual solder bath. This soldering technique has therefore the largest temperature gradients and is the most difficult to process. Minimum degradation of the insulation resistance of MLCs as a result of thermal shock with a low temperature solder wave, high assembly bottom preheat temperatures, and moderate belt speeds of 1.2 to 1.5 meters/minute are recommended. The actual solder wave temperature should be 232°±2°C for 60Sn/40Pb solder and the assembly bottom preheat should exceed 140°C with a dwell time of the components not to exceed 10 seconds; a recommended wave solder profile is shown in Figure 9.

232°C WAVE TEMPERATURE

100°C MAXIMUM, 70-80°C PREFERRED

160°C

FIRST WAVE

SECOND WAVE

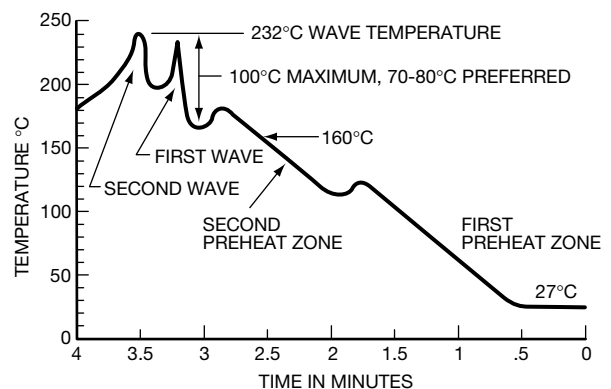SECOND PREHEAT ZONE

FIRST PREHEAT ZONE

27°C

Figure 9. Wave Soldering Profile for Minimum Thermal Shock

The key to bottom side assembly preheat is that the top side of the assembly not be heated and this can be accomplished by proper choice of type of preheating. Area panel heaters offer the best choice as these heaters are close for direct preheating but minimum convective heating[4].

In all three soldering techniques described above, temperature profiling is critical and this in itself is important for process control.

Post Solder Handling

Post solder handling includes testing, depanelization, installing connectors, and putting in a chasis. These operations constitute another large source of defects in MLCs and is one of the least understood as far as specifications are concerned. It is essential that board deflections in any of these operations be reviewed and evaluated in terms of the resultant stresses on all components including MLCs. Estimates show that a maximum of 0.1mm deflection for each cm of board segment or 3mm for 10cm board segment may be allowed. Components also need to be isolated from connectors, mounting holes, and pots to minimize damage from deflections which may occur during board handling; typical board warpage cracks are shown schematically in Figure 10.

In many cases, boards are built on a multipanel assembly for mass soldering and then are depanelized. Various methods are used for depanelization, but the low mechanical stress techniques[2] are high speed fine-tooth saws with rigid fixturing and linear cuts, laser cutting of thin boards, and water jet technique. Pre-routing of boards help limit the board deflection during depanelization.

Thermal and Mechanical Properties of MLCs

As clearly demonstrated earlier[5,6], the mechanical and thermal shock resistance parameters of MLCs are important for understanding the SMT applications of these devices. In particular, it was shown that thermal stresses resulting from rapid changes in temperature (for example, wave soldering of MLCs) can explain the thermal shock properties of these capacitors. These thermal stresses σ_s can be defined by:

$$\sigma_s \ = \ \frac{E\propto}{(1\text{-}\mu)} \quad \frac{s\varnothing t^2}{(k/dc_p)} \quad ....(1)$$

Where E is the elastic modulus, $\propto$ is coefficient of linear thermal expansion, s is the shape factor, $\varnothing$ is the rate of change of temperature, t is the overall thickness, μ is the Poisson's ratio, and (k/dc_p) is the thermal diffusivity with k, d, and c_p being the thermal conductivity, density, and specific heat respectively. As equation (1) suggests, and as a number of analytical studies have shown[7,8], materials with lower E, lower $\propto$ and lower μ along with higher thermal diffusivity are desirable. The above equation clearly suggests that lower rates of change of temperature and thinner geometrics are desirable. For this reason, proper preheat, for example, in wave solder as well as in IR and vapor phase soldering techniques is so critical. The thermal stresses by themselves are not sufficient for failure to occur: crack initiation and crack propagation, and the corresponding thermal stress resistance parameters R' and R" play an
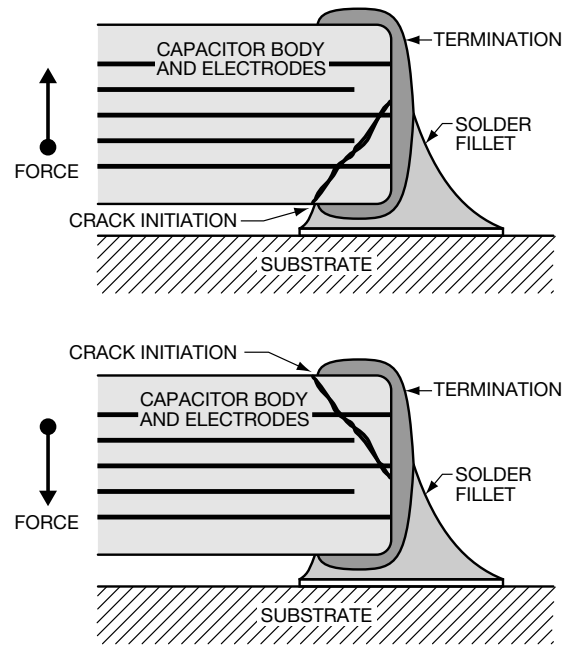

Figure 10. Typical Board Warpage Cracks

important role in the thermal shock behavior of chips[8]. Further evaluation of dielectric materials[9] shows that parameters like thermal diffusivities show significant changes to effect thermal stresses and may be utilized to improve the thermal shock behavior of MLCs. The σ_s, R', and R" parameters are dependent on the material characteristics such as homogenity, porosity, and pre-existing flaws, and this makes the analysis very complex. Considering that the failure criterion of fracture occurs when the thermal stress reaches the fracture stress, it is possible to estimate the maximum temperature difference which a sample can withstand, and this temperature difference is directly proportional to R' and inversely proportional to half the sample thickness t and to the surface heat transfer coefficient h. Examples will be shown below to isolate some of the parameters mentioned above and show their effect on thermal shock behavior of MLCs.

Experimental Procedure

Selected examples of experiments and their results are shown to isolate various parameters listed in equation (1) where thermal stresses depend on square of the overall thickness, the rates of change of temperature, and wetting characteristics of the termination. The complexity of this study is further shown by evaluating materials with varying K_{1c} and stresses in the termination itself.

Parts are tested by carrying out life tests and 85°C/85%RH testing of parts mounted on substrates using wave solder technique.

Ceramic Dielectrics Evaluated

In an effort to isolate various parameters mentioned above, experiments were carried out with dielectric ceramic materials classified by E1A as X7R and Z5U.

(i) *Dependence of Fracture Toughness, K_{1c}*: MLCs were prepared with $BaTiO_3$ based X7R formulations referred to as ceramic A and ceramic B and their K_{1c} values were determined using the Vicker's microin-

dentation technique[10]. Samples were also prepared with Z5U ceramics C and D.

(ii) *Thickness Dependence:* MLCs of varying thickness were prepared with ceramic B above to study the effect on σ_s.

Effect of Termination

It has been shown earlier[5] that MLCs with Pd/Ag termination and plated terminations show large differences in thermal shock due to the rate at which the heat transfer occurs across the termination. In this paper, other parameters which effect the termination are investigated:

(i) *Effect of Glass Frit in the Termination:* Composition of a termination used in MLCs (made from Ceramic C) was altered with glass frit and its effect will be shown.

(ii) *Effect of Residual Stress in Termination:* Ni barrier plated in two different plating baths with varying pH was investigated, and the resultant stresses in the Ni film were systematically varied. These stresses are measured and their effects are shown.

Thermal Stress Evaluation Test Method

The wave solder test technique has been described in detail in an earlier publication[5] and this was used to evaluate the effect of thermal stresses. Briefly, it consists of mounting MLCs on FR4 boards using an epoxy and soldering parts with no preheat at belt speeds of 3 meters/minute using 60 Sn/40Pb solder at 260° ±5°C.

Life and 85°C/85% RH Testing

MLCs reflowed after wave soldering were tested at 125°C using twice rated bias voltage of 100 volts. In addition, in selected cases these devices were tested at 140°C and eight times rated voltage of 400 volts. Other groups of these devices were tested at 85°C/85% RH with a bias voltage of 100 volts.

Results and Discussion

Effect of Fracture Toughness, K_{1c}

In Table 1, thermal shock results are shown for 1206 0.001 μF X7R chips made from ceramic A with K_{1c} value of 1.3 MPa.m$^{1/2}$ and from ceramic B with K_{1c} value of 0.9 MPa.m$^{1/2}$ respectively.

As the results in the last column clearly show, the susceptibility to thermal shock changes from no failures to MLCs showing about 75% failure rate. This clearly demonstrates that ceramic materials with higher K_{1c} are desirable.

Effect of Chip Thickness

In Table 2, thermal shock results are shown for Z5U ceramic D as a function of thickness. The table shows that (for a chip style) as the thickness increases, the

number of failures increase rapidly and as the chip size increases, this increase is faster because σ_s is also proportional to $\Delta \propto$ (difference in coefficient of thermal expansion between the metal and ceramic).

Table 2. Effect of Chip Thickness on Thermal Shock

	Ceramic D Overall Chip Thickness (mm)		
	0.5	1.0	1.5
Chip Style	Thermal Shock Failures (% Failures)		
1206	0	0	3
1210	0	2	24
1812	0	11	41

Effect of Termination

(i) *Wetting Characteristics:* It was shown in an earlier work[5] that MLCs with plated terminations wet about a hundred times faster compared to MLCs with Pd/Ag or Ag terminations. This in turn demonstrated that the rate of heat transfer ∅ can be varied to the extent that Ni plated parts had ~ 100% failures whereas standard thick film terminations of Ag and Pd/Ag had no failures when subjected to the thermal shock testing; this result is shown in Table 3.

Table 3. Effect of Wetting Characteristics on Thermal Shock

1210 Chips Ceramic C 0.1 μF 1.55mm Thick		
Ag Termination	Ag with Plated Ni Termination	Ag with Ni Treated at 400°C for 1 Hr.
0/200*	199/200*	0/200*

(*Number of Failures to Total Number Tested)

To demonstrate that this result was indeed a result of the Ni wetting characteristics, the Ni layer was oxidized while still maintaining excellent adhesion to the chip termination and the number was zero again. This result was obscured by the possibility that there are residual stresses in the Ni film.

(ii) *Residual Stresses in the Ni Film:* MLCs made with ceramic B which had a low K_{1c} were plated in two different types of Ni baths P and Q with varying pH values. Change in the pH results in different residual stresses in the Ni film, and these stresses are measured by a gearless contractometer.

Samples are then tested for susceptibility to thermal shock and as the results show in Table 4 the number of thermal shock failures is independent of these

Table 1. Effect of K_{1c} on Thermal Shock

Chip Style	Capacitance Value (μF)	Ceramic Type	Chip Thickness (mm)	K_{1c} (MPa.m½)	Thermal Shock*
1206	0.001	A	0.85	1.3	0/50
1206	0.001	B	0.85	0.9	37/50

stresses within the range of stresses measured. This result clearly demonstrates that the conclusion arrived at earlier regarding the wetting characteristics and rate of heat transfer is the dominating parameter.

Table 4. Effect of Residual Stresses in Ni Film on Thermal Shock

Group	Ni Bath Type	pH	Tensile Residual Stresses in Ni Film (MPa)	Thermal Shock Failures (%)
1	P	2.9	0	6.6
		4.5	13	5.4
		5.0	76	6.6
I	Q	3.0	328	3.8
		4.1	119	2.9
		5.5	77	3.3

(iii) *Glass Frit Content of Termination:* The thermal shock behavior of chips may be changed by increasing the amount of glass frit in the Ag termination. Results in Table 5 show the results of two ceramics having lower K_{1c} values purposely chosen to have chips with higher thermal shock failure rates so that the effect of glass frits may be evaluated.

Table 5. Effect of Glass Frit in Termination on Thermal Shock

Chip Type	Ceramic B 1206 0.1 µF	Ceramic C 1825 1.0 µF
Conc. of Glass Frit (Weight %)	Thermal Shock (Failures %)	
2.7	54	56
4.3	41	24
5.0	35	22

In both cases, as the amount of glass frit increases, the thermal shock failure rate drops; and this is attributed to lower thermal conductivity of the termination. This is deduced from the observation that the glass frit is distributed along the grain boundaries of the termination Ag and its behavior is dominated by the glass frit which has a thermal conductivity of about 1 w/m°K compared to silver whose thermal conductivity is about 400 w/m°K. It should be noted that the porosity in all cases is about the same.

Life Test and 85°C/85% RH Results

Detailed experiments like the ones shown can be carried out to optimize the K_{1c} values, the chip thickness, the wetting characteristics of the termination, the residual stress in the Ni film, and the glass frit in the termination to build MLCs for surface mount assemblies exhibiting very low failure rates. This is demonstrated by mounting chips on experimental surface mount boards, subjecting them to wave solder processing, and subjecting them to accelerated life testing at 100V, 125°C or highly accelerated life testing at 400V, 140°C followed by 85°C/85% RH. Results of some of these tests are reported in an earlier publication[6]. Models on conduction and failure mechanisms published earlier[11]

show that voltage and temperature acceleration factors can be used to predict component failure rates at use conditions of, for example, 65°C, 25V (a conservative use condition; actual use voltages are usually 5 or 12 volts). In the tests listed above, 100 piece samples nominally show 0 or 1 failure and the failure may occur after 10 to 20 minutes of testing.

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left[\frac{E_s}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right]........(2)$$

The time to failure t, temperature T, and voltage V may be estimated from an empirical relation arrived at by Prokopowicz and Vaskas[12] where E_s is the pseudo-activation energy, k is the Boltzmann's constant and n is the voltage exponent. In our experiments, $E_s \sim 1.8$-$1.9e$ V for various dielectrics, n ~ 3 and accelerated test voltage and temperature are 400 volts and 140°C respectively. This equation (2) suggests that the failure occurring after only 1.0 minute under accelerated test conditions mentioned above will fail after 39 years in the use conditions also mentioned above or the failure rate is sub-ppm; as noted above, actual failures occur after 10 to 20 minutes of testing, and therefore the failure rates are very low.

The various results demonstrate the capability of the model where a few parts of this complex study can be used to improve the reliability of MLCs at the board level.

Conclusions

In this paper, various aspects of the surface mount applications of MLCs have been outlined. These consist of:

A. Zero Defect Soldering Designs

B. Pick-and-Place Considerations

C. Soldering Techniques

D. Post Soldering Handling

E. Thermal and Mechanical Properties of MLCs

An understanding of the thermal and mechanical properties of MLCs along with key elements of the model where the thickness of MLCs, the fracture toughness of ceramics, and the role of terminations are optimized and allow us to redesign these devices. With this redesign, it is shown that failure rates of MLCs in various surface mount assembly operations are at sub-ppm levels.

Acknowledgement

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