TECHNICAL PAPER

So Many Electrons, So Little Time... The Need for Low Inductance Capacitors

John Galvagni
Sara Randall
Paul Roughan
Allen Templeton

KYOCERA AVX Components Corporation
17th Ave. South
Myrtle Beach, SC 29578

Abstract

High di/dt ratios, large current pulses over short times, are an inevitable part of today's fast electronic circuitry. They can cause high voltage spikes when passing through paths that have inductance. The task of the designer then, is to have high energies available, but not the associated voltage excursions, by reducing the total inductance. Eliminating wire bonds, reducing path lengths, and using low inductance components is the regimen.

This paper describes the availability of capacitors that can go a long way to providing the energies needed, but simultaneously, lower the intrinsic inductance it contributes. We will review the source of the inductance, the current components available, and other advances that will give the designer a more useful menu.

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THE NEED FOR LOW INDUCTANCE CAPACITORS

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1. Introduction

Current flow during the simultaneous switching of logic gates in digital circuits causes voltage fluctuations to be generated across power supply buses. The magnitude of these fluctuations depends upon the amount of current, the rise times, and the effective chip and package inductance. This power supply noise can couple through a logic circuit driver and appear as a spurious voltage signal on the input terminals of a logic receiver circuit, sometimes causing logic switching errors.

The trend in the electronic industry is toward higher frequency switching, decreased pulse rise times and increased circuit density. This trend exacerbates the simultaneous switching problem to the point that it can become a serious limitation to improved system performance.

The most common way to manage this noise problem is to use capacitors that act as local energy sources to provide the voltage required to switch and refresh logic gates. These capacitors are "decoupled," or temporarily independent from, the power supply with its associated noise spikes, and from the package inductance. However, the decoupling capacitors themselves can generate voltage spikes, given by:

$$V = L \ (di/dt)$$

where L is the inductance of the capacitor. Thus, in high frequency systems, where (di/dt) can be quite large, the size of the voltage spike can only be reduced by reducing L.

The LICA® (Low Inductance Capacitor Arrays) product line was developed as an extension of work done with IBM on their DCAP® [1, 2] to address that problem. Figure 1 shows the basic construction of these parts, while Figure 2 depicts the internal electrode-tab arrangements. Because of its unique construction, the device has a very low inductance, (A later section will detail this.) A typical LICA® decoupling capacitor exhibits an inductance of 60 picohenries, an order of magnitude lower than that attainable even with low inductance capacitors such as the 0612 or 0508.

2. Applications

The basic LICA® design allows a wide range of parameter variation which makes the device a truly application-specific decoupling capacitor. A few examples are as follows:

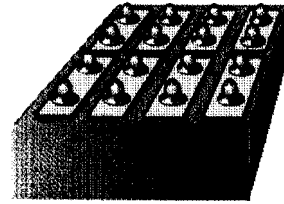2.1 LICA® can be configured as a single capacitor unit, or as an array of 2, 4 or 8 capacitors in a single

Fig. 1: LICA® Shown here is the four-capacitor array using the C4 termination. Each capacitor has four terminals.

body. All options are 1.60mm wide by 1.85mm long. The quad cap array is especially useful for decoupling ECL (emitter-coupled logic) circuits, since this logic family normally requires three different supply voltages and ground. One quad LICA® can decouple all three voltages.

2.2 High density CMOS logic circuits typically are powered by a single voltage and generate high switching currents over very short rise times. A single capacitor LICA® is the best choice for this application, providing five times the capacitance of the quad device.

2.3 LICA® product is currently built using standard EIA dielectrics such as X7R, Z5U and Y5V. A specially developed dielectric is also available which delivers its
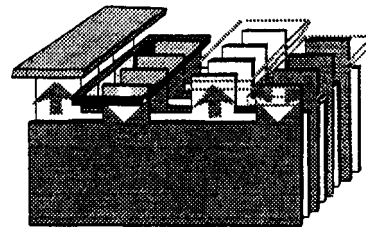

Fig. 2: Electrodes & Tabs. The internal sections of each capacitor is depicted. The arrows indicate the direction of the currents which effect the inductance.

maximum capacitance at 60°C. These dielectrics are compared in Figure 3. Many of the newly developed microprocessor chips run well above room temperature during operation.
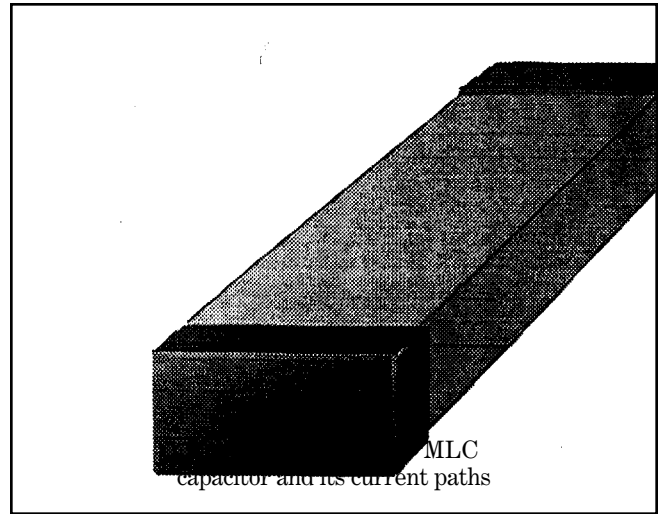
2.4 Presently the available voltage rating is 25 volts. Work is in process to develop 16V rated parts (higher capacitance), which will be in higher demand as the industry moves toward lower-voltage (3V) operating systems.

2.5 The basic LICA® part uses C4 solder bumps for flip-chip attachment. This technique offers the ultimate in low inductance since it results in many current injection points. The device is also available with thin film (Al, Au) metallized contacts. Both of these termination techniques are particularly useful for MCM application. Note that wire bonding of these devices is not recommended - each millimeter length of one-mil diameter gold wire contributes 1,000 picohenries of inductance, 20 times larger than the capacitive inductance.

2.6 Parts are available in four body thicknesses - 0.875, 0.750, 0.650 and 0.540 mm. C4 solder bumps add 0.1mm to the overall thickness. The thinner parts were designed to be comparable to silicon chip thicknesses, especially useful in MCM applications where the IC chip is recessed into cavities in the substrate, sometimes referred to as the "chip first" process.

3. Low Inductance by Internal Design

LICA® achieves low inductance from its small size and the direction of the electrode current flow required to charge the dielectric. In a standard surface mount capacitor (Figure 4), the charging current flows from one termination down the electrode into the dielectric and out into the counter electrode. The total path of the port current, i.e.– the length of the capacitor, determines the inductance. The inductance of 0603 and 0805 surface mount capacitor for example, is less than that of

MLC capacitor and its current paths

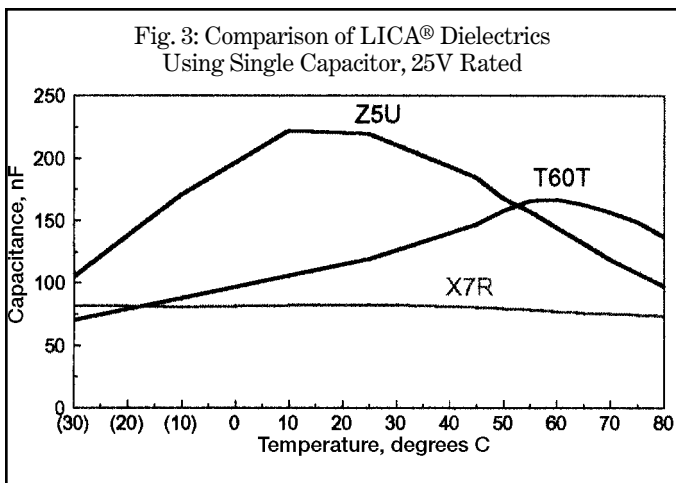inductance of a plate *and do not address mutual inductance coupling between electrodes.*

The current in adjacent electrodes flows in the same direction and results in a mutual inductance term that increases the overall inductance of the capacitor. AVX has published several technical information articles on advanced decoupling that address this topic. [3,4] In the past AVX has designed several large decoupling capacitors that have minimal inductance because the current in adjacent electrodes flows in opposite direction. This reduces the mutual inductance and minimizes the effective path length of the charging current.

This is the same idea behind the original DCAP® design by IBM. The charging current flowing out on the positive plate returns in the opposite direction along the adjacent negative plate; this minimizes the mutual inductance. The arrows in Figure 2 depict this. Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

To better understand these complicated electromagnetic interactions within multilayer ceramic capacitors, AVX has funded an ongoing numerical modeling research project at the University of South Carolina Department of Electrical and Computer Engineering since 1991. The current version of the electromagnetic (EM) CAD tool calculates the potential distribution inside the capacitor.

$$\nabla \cdot \left(\left\{ \begin{matrix} \varepsilon\ (x,y,z) \\ \sigma\ (x,y,z) \end{matrix} \right\} \nabla \phi \right) = 0$$

From the potential distribution, the surface charge density on each electrode is obtained. At the frequency of interest, the current continuity equation relates the conduction currents flowing on each plate to the surface charge density, or displacement currents flowing into

Fig. 3: Comparison of LICA® Dielectrics Using Single Capacitor, 25V Rated

the 1206 size. The aspect ratio of the electrodes has a second order inductance effect: a 1210 case size design has lower inductance than a 1206. AVX designs lower inductance surface mount capacitors by terminating the electrodes along the longest side producing an 0612 instead of 1206, and 0508 instead of 0805. The first order effect of length is reduced and the second order aspect ratio is dramatically improved as well. These empirical design improvements are drawn from the simple self

and out of the dielectric. Once all of the conduction current vectors are solved, the total inductance, both self

$$\nabla \cdot \vec{J} = -j\omega \, \rho_s$$

and mutual inductances, can finally be calculated by the concept of partial inductance:

With this tool, designs tradeoffs to minimize inductance can be explored quickly to meet customer design requirements.[5]

In addition to needing new modeling tools to fully understand LICA® designs, new test fixturing for measuring inductance is required. Since the LICA® is terminated on the same side of the part, our standard surface mount capacitors testing fixtures were useless. The need to minimize fixture parasitics is also critical. The method chosen was to directly probe the inverted LICA® using a Cascade Microtech RF probe and read the complex impedance using a Wiltron Vector Network Analyzer. The Cascade probe is calibrated using a reference substrate consisting of an open, short and 50 ohm standard. With the phase reference of the network analyzer set at the tips of the probe, the complex impedance of the LICA® is displayed on a Smith Chart. The first order approximation to the inductance is determined from the "self resonant frequency" (SRF) of the LICA®. This is the frequency at which the impedance passes from the lower capacitive region of the Smith Chart to the inductive upper region through the 0-j axis near zero. Another method is to look at the actual impedance reading over a small frequency region and assuming that the capacitance stays constant, the inductance can be calculated by the shift or slide in the reactive impedance.

4. Preserving the Low Inductance Through Attachment

The new arrangements of the internal electrode demanded a different approach to terminations as well. Although mainly required to achieve the proper "injection points", the fine line geometry required on today's dense packaging created a situation where the usual thick film terminations would not work. Thin film systems had long since demonstrated the resolutions and the material versatility needed, but the combination with dielectric ceramics was particularly challenging. Thin film deposition schemes require substrates with very smooth surfaces that can be patterned using photolithography techniques on individual parts which were in a precise array. The typical ceramic capacitor had neither of those attributes, and so required a large amount of development.

The terminations on LICA® devices need to provide interconnections between the part and substrate that have low resistance and low inductance, as well as adequate mechanical strength. Other factors important in the selection of an interconnection technique include relative interconnect density, reliability, thermal performance, corrosion behavior, reworkability, turnaround time, cost, and manufacturing capability. Figure 4 shows the current variations. *Table 1 compares the key parameters of the different styles.*

4.1 Originally, terminations on the DCAP® array used controlled collapse chip connection (C4) technology. (as shown in Figure 1) This termination scheme minimizes both interconnect inductance and use of valuable board real estate. The C4 joining process was developed by IBM Corporation in the early 1960's for their solid logic technology (SLT) system [6]. The C4 technique is complex, involving the layered deposition of several different metals, typically through a metal shadow mask. The initial metal layers are deposited to limit the spread of solder on the top surface of the chip and are referred to as ball limiting metallurgy (BLM). The BLM is also designed to provide adhesion of the metal termination to the multilayer ceramic LICA® part. The final layer deposited is a lead-tin solder that is evaporated onto the BLM. The deposited solder is then reflowed at 350°C in a reducing atmosphere. To minimize surface energy the molten solder forms a sphere on each of the BLM pads. An interconnection between substrate and part is made by turning the part upside down, aligning it to its mating substrate, and joining the two by again reflowing the solder.

There are a few companies equipped and licensed to use C4 technology. However, many companies are not tooled to use this complex and expensive technique and need termination schemes that are compatible with the assembly processes they use. In response to this, AVX is developing alternative termination schemes to meet these needs. These efforts are focused on the interconnection methods that are currently used on multicomponent modules (MCM's), including wirebonding, tape automated bonding (TAB) techniques, and gold ball flip chip bonding. A comparison of the four primary interconnection techniques used on MCM's and being adapted to LICA® is given in Table 1.

4.2 Automated wirebonding techniques are fast, simple, efficient, and reliable. Bonding pads are sputter deposited on the top of the LICA® part. Typically the material deposited is either aluminum or a multilayered structure consisting of a chromium adhesion layer followed by a gold bonding layer. The back side of the part is die-bonded to the substrate with metals and/or adhesives. Gold wirebonds are then made, one at a time, from the part to the substrate. Practical constraints generally limit wirebonding to pads on the periphery of the device. With the new MCM's however, this attachment technique totally voids the advantage of using low inductance components. A significant amount of additional board real estate is also consumed by the wire bonds. Therefore techniques that have higher interconnection densities, preserve the low inductance integrity, and make all bonds simultaneously, such as TAB, C4, and gold bump bonding, are replacing wirebonding.

4.3 Interconnections made using TAB generally have

an improved electrical and thermal performance relative to wirebonding [7]. The TAB process involves bonding a thin polymer tape that contains metallic circuitry to a bumped chip using modified wirebonding equipment. Each bump is made by thermosonically bonding a gold ball to a metallized pad. The metallized pads on each part are produced by the thin film deposition of an adhesion layer (Cr), followed by a barrier layer (Cu), and finally a bonding layer (Au). Interconnections between the tape and the part, called inner lead bonds (ILB), are made by thermocompression bonding. Connections from the tape to the substrate, called outer lead bonds (OLB), are made by soldering or thermocompression bonding. As with wirebonding, TAB is generally limited to

C4 (Flip Chip)

Gold Plated TABS

Gold Bumps

Thin Film

Fig. 5: Termination Options
Shown above are the current options for interconnect systems on the LICA® (dual) capacitor

peripheral interconnections. Thus, these techniques are limited to the single and double capacitor designs of LICA® (higher order LICA® designs require interconnections from the center of the part). The TAB technique is an attractive option for MCM assembly since components can be pretested on tape prior to incorporation into the module. The TAB interconnections typically exhibit a lower inductance relative to wirebonding, but a higher inductance relative to the flip-chip methods of C4 and gold ball bonding.

4.4 Gold bumping is currently being developed in order to overcome the limitations of the previous techniques [8]. This method utilizes conventional wirebonding equipment to put gold balls on termination pads on the LICA® part. The termination pads consist of the same metallization that is used for wirebonding. As in wirebonding, a ball is formed at the tip of the wire via electric discharge. This gold ball is then thermosonically bonded onto the termination pad. The wire is then clamped and pulled until it breaks. This leaves a gold ball on the surface. The wire used in gold ball bonding is alloyed with a small amount of palladium to reduce the elongation of the wire. This is designed to make the wire break at a consistent distance above the gold ball. A coining tool is then used to level the tops of the gold balls. Interconnections between the part and substrate are made using thermocompression and/or thermosonic bonding.

4.5 Some interesting work is being done using thin film (Aluminum) terminations on LICA®. With the so-called "chip first" technique, the LICA®, along with the semi-conductor die, are placed in cavities in a substrate, such that their termination surfaces are co-planar with the substrate surface. A photodefinable polymer is deposited on the surface and via holes are etched, exposing the chip bonding pads. The interconnect metal is then deposited and patterned.

4.6 While the development efforts at AVX are currently concentrating on providing C4, wirebonding, TAB, and gold bump bonding terminations on LICA® parts, the next generation of LICA® terminations may include new interconnection techniques such as ball grid arrays (BGA) [9] and thin film gold-tin stratified structures [10].

5. Summary

Within the increase in circuit speeds, and the concurrent continued miniaturization of circuitry with the MCM evolution, a very different ceramic capacitor is demanded. The LICA® capacitor fills that void with a device which is very low in inductance, efficiently designed to use little space, and is compatible with most interconnection systems. Unlike other new components, however, this one comes with several years of experience, and a demonstrated history of manufacturing and reliability.
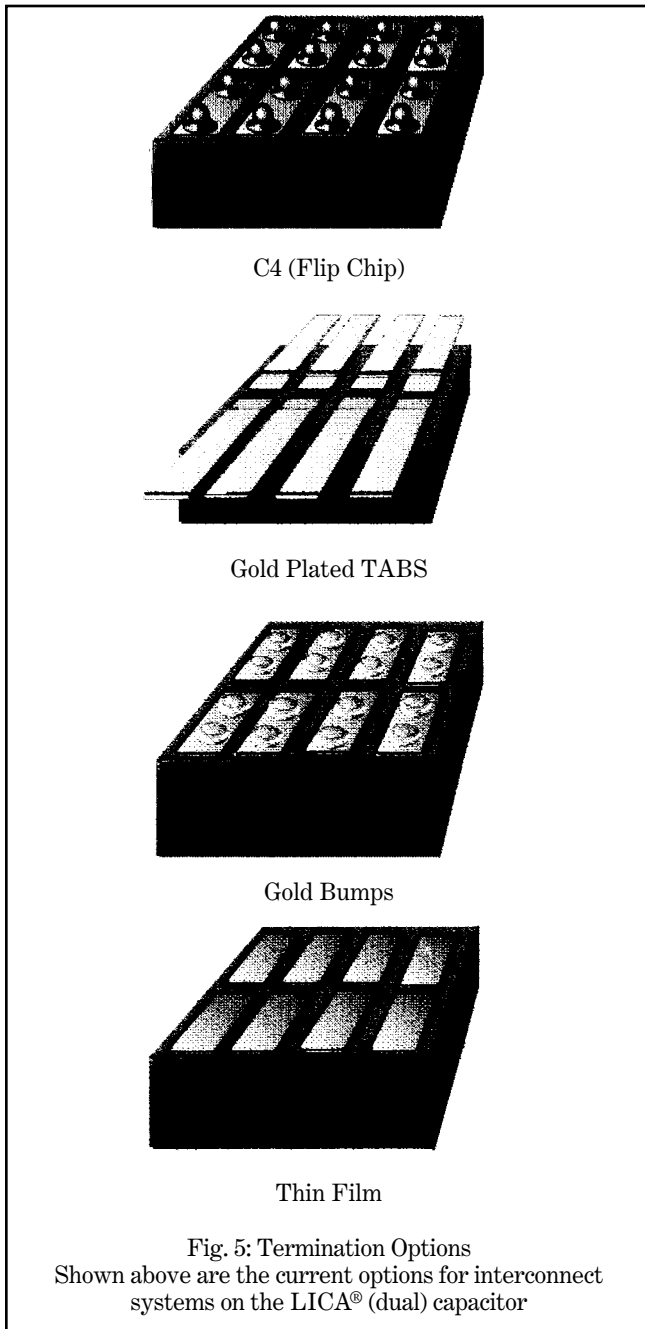
Technique	Wirebonding	C4	TAB	Gold Bump	Thin Film
Table 1: Comparison of interconnection techniques					
Advantages	Well established Well understood Low cost	Minimize inductance Minimize space needed Easy to rework	Pretestibility	Minimize inductance Minimize space needed	Least expensive High volumetric efficiency Low process temperature
Disadvantages	Requires significant additional real estate around component Increased inductance	Complex Expensive Difficult to inspect connections	Requires additional real estate around component Added process steps Increased inductance Hard to rework	New technique	Requires advanced techniques Least forgiving of thermal mismatch
Typical Materials	Au, Al	Pb-Sn	Cu, Au, Al polyimide	Au-Pd	Al
Typical Process	Wirebond	Reflow	Thermocompression	Modified Wirebond, Thermocompression	Chip First Multilayer interconnects
Typical Process Temperature	105°C Ultrasonic	350°C	550°C Pulsed	250°C Ultrasonic	<125°C
Relative Cost	5	25	50	8	2
Relative Inductance	very high	low	moderate	low	low
Termination provided on LICA®	A1 or Cr/Au pad	BLM and solder balls	Cr-Cu-Au pads, Au bumps, ILB TAB tape	Cr-Au pads and Au bumps	Al pads

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NORTH AMERICA
Tel: +1 864-967-2150

ASIA
Tel: +65 6286-7555

CENTRAL AMERICA
Tel: +55 11-46881960

EUROPE
Tel: +44 1276-697000

JAPAN
Tel: +81 740-321250

WWW.KYOCERA-AVX.COM