

# TECHNICAL PAPER

## Electrostatic Protection Using Ceramic Capacitors

**Oliver Zimmermann**

**John McCarry**

*KYOCERA AVX Components Corporation*

One AVX Boulevard

Fountain Inn, S.C. 29644 USA

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### **Abstract**

Any conductive interface between an electrical circuit and the outside world introduces the possibility of damage through electrostatic discharge (ESD). Accumulated static charge on a person, a cable, or any similar surface can readily dissipate its stored potential energy upon contact into sensitive components resulting in highly destructive currents.

## ELECTROSTATIC PROTECTION USING CERAMIC CAPACITORS

### TRADITIONAL ELECTROSTATIC PROTECTION

Any conductive interface between an electrical circuit and the outside world introduces the possibility of damage through electrostatic discharge (ESD). Accumulated static charge on a person, a cable, or any similar surface can readily dissipate its stored potential energy upon contact into sensitive components resulting in highly destructive currents. These voltages can reach the kilovolts and require the addition of specialized circuits and semiconductor devices to protect downstream circuits and ensure continued reliable operation.

Traditional protection devices include a myriad of different varistors and transient voltage suppression (TVS) diodes. Both operate on the principle of shunting current to ground when the applied voltage exceeds a clamping threshold as shown in figure 1.

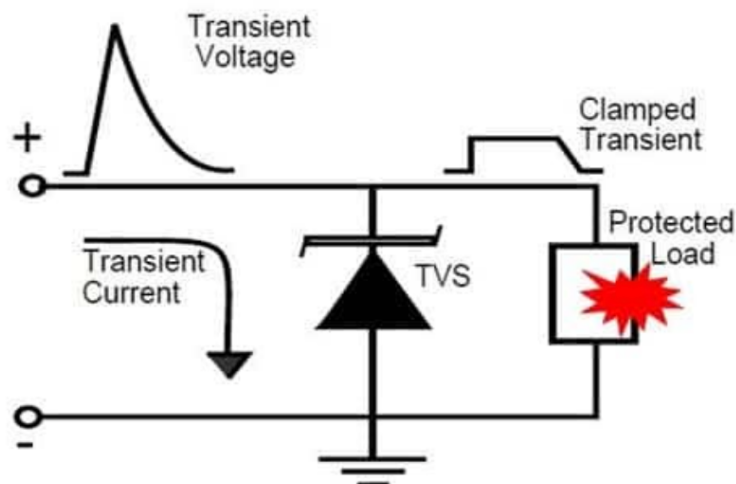


Figure 1 - TVS diode used to shunt high voltage current to ground (Tech Design)

Ideally, varistors and TVS diodes only activate to protect the circuit when a high voltage is present and impart no parasitic effects during normal operation. For high-speed data lines, in particular, it is critical that the protection device introduce as little capacitance as possible (Electronic Design). TVS diodes and varistors are therefore specified not only by their voltage ratings, but also by their capacitance, leakage current, and package options.

This article explains the functional properties of ceramic capacitors as alternative overvoltage protection, the key design considerations of multi-layer ceramic capacitors, and finishes with a case study to illustrate these principles.

# ELECTROSTATIC PROTECTION USING CERAMIC CAPACITORS

## CERAMIC CAPACITORS AS AN ALTERNATIVE

In practice, many input/output (I/O) lines are not high-speed and can tolerate a fair amount of parasitic capacitance. In these scenarios, a specialized device can be used to gain a significant cost advantage over traditional TVS diodes and varistors: the ESD-safe multi-layer ceramic capacitor (MLCC).

These capacitors contain specialized structures that allow them to tolerate voltage impulses orders of magnitude higher than their continuous DC rating. Examples of X7R devices are shown in table 1. As can be seen, a common 25 V 0805 chip capacitor in this series can withstand 26 kV of ESD.

### ESD-SAFE™ X7R RANGE

Capacitance		0603				0805						Q1206					
Code	Value	50V		100V		25V		50V		100V		25V		50V		100V	
472	4.7 (nF)	18kV	G	18kV	G	18kV	N	18kV	N	18kV	N	20kV	Q	20kV	Q	20kV	Q
682	6.8	18kV	G	18kV	G	18kV	N	18kV	N	18kV	N	20kV	Q	20kV	Q	20kV	Q
103	10	18kV	G	18kV	G	18kV	N	18kV	N	18kV	N	20kV	Q	20kV	Q	20kV	Q
153	15	20kV	G			20kV	N	20kV	N	20kV	N	22kV	Q	22kV	Q	22kV	Q
223	22	20kV	G			22kV	N	22kV	N	22kV	N	24kV	Q	24kV	Q	24kV	Q
333	33	20kV	G			22kV	N	22kV	N	22kV	N	24kV	Q	24kV	Q	24kV	Q
473	47	22kV	G			22kV	N	22kV	N	22kV	N	26kV	Q	26kV	Q	26kV	Q
683	68	22kV	G			24kV	N	24kV	N	24kV	N	26kV	Q	26kV	Q	26kV	Q
104	100	24kV	G			24kV	N	24kV	N	24kV	N	26kV	Q	26kV	Q	26kV	Q
154	150					24kV	N	24kV	N	24kV	N	28kV	Q	28kV	Q	28kV	Q
224	220					26kV	N	26kV	N	26kV	N	28kV	Q	28kV	Q	28kV	Q
334	330					26kV	N	26kV	N	26kV	N	28kV	Q	28kV	Q	28kV	Q
474	470					26kV	N	26kV	N	26kV	N	28kV	Q	28kV	Q	28kV	Q
684	680					26kV	N					28kV	Q	28kV	Q	28kV	Q
105	1 (μF)					26kV	N					28kV	Q	28kV	Q	28kV	Q
155	1.5											30kV	Q				
255	2.2											30kV	Q				

Table 1 - ESD-Safe MLCC's from KYOCERA AVX

To understand the protection principle behind using these capacitors, consider the typical ESD test circuit shown in figure 2 for the human body model.  $R_c$ ,  $C_d$ , and  $R_d$  are specified by the test standard.  $C_x$  is the ESD-Safe capacitor added across the device to be protected.

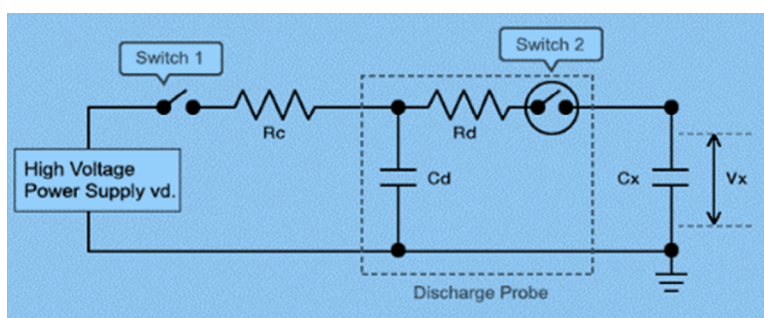


Figure 2 - Human body ESD test model with ESD-safe  $C_x$  added for protection

## ELECTROSTATIC PROTECTION USING CERAMIC CAPACITORS

### CERAMIC CAPACITORS AS AN ALTERNATIVE

Since  $C_x$  is able to safely withstand extremely high ESD voltages, the final voltage ( $V_x$ ) that will be seen by the downstream circuit will simply be the result of capacitive charge sharing between  $C_d$  and  $C_x$ . As shown in equation 1, the final output voltage  $V_x$  will be significantly reduced by the addition of  $C_x$ .

If  $C_x$  is much larger than  $C_d$ , the voltage reduction is substantial. This simple mechanism provides adequate ESD protection for many I/O lines that are insensitive to the added capacitance. In addition, both cost and space savings are often realized.

$$V_x = \frac{C_d}{C_d + C_x} V_d$$

*Equation 1 - Final output voltage  $V_x$  when protective capacitor  $C_x$  is added*

### DESIGN CONSIDERATIONS FOR MLCC PROTECTION

Unlike varistors or TVS diodes, there is no clamping voltage or maximum peak voltage defined for the ESD-safe MLCC. Although the use of ESD-safe protection capacitors can be an effective practice, engineers often overestimate the capacitor's performance by ignoring its inherent degradation with applied voltage. Generally speaking, the amount of capacitance drop for NPO dielectrics is negligible. However, the amount of capacitance drop for X7R capacitors can be in the 50% range or even greater. Furthermore, the capacitance drop varies from manufacturer to manufacturer and depends on the material composition used for the X7R dielectric. This drop-in capacitance from the expected value of an X7R capacitor can result in a much higher voltage seen by the IC or device to be protected.

As an example, let us consider a 1 nF MLCC used in a circuit with the requirement of 8kV contact discharge based on an ESD model capacitor of 150 pF. Using an MLCC with NPO dielectric would result in a theoretically calculated voltage of approximately 1044 volts. On the other hand, using a 1 nF capacitor with X7R dielectric which has a 50% drop in capacitance the voltage  $V_x$  across the capacitor will approach 1846 volts.

One might simply hope to use NPO capacitors for all their MLCC protection needs. Unfortunately, NPO MLCCs are limited in their available maximum capacitance value due to the low dielectric constants. For this reason, in many cases, MLCCs with X7R dielectric must be used to provide sufficient ESD protection.

### ESD ROBUSTNESS OF MLCC

When used for protection against ESD, the MLCC acts as a capacitive voltage divider. The charge of the ESD pulse is distributed among the capacitive layers, and as the number of active electrodes increases, the robustness of the device follows. In addition, increased thickness of each layer helps to improve the voltage that can be withstood.

As such, the generalized rule is that to maximize MLCC robustness for ESD protection, the designer should incorporate the largest possible capacitance in the largest possible case size to achieve the greatest number of total dielectric layers with maximal thickness.

# ELECTROSTATIC PROTECTION USING CERAMIC CAPACITORS

## ESD ROBUSTNESS OF MLCC

To demonstrate this, KYOCERA AVX carried out ESD robustness tests on a variety of capacitors using the AECQ 200, IEC61000-4-2, and ISO10605 standards. For each run, ten samples of the part were tested. If any single part failed, then the ESD voltage was lowered and ten new parts were tested. Table 2 summarizes these tests for several different 0603 MLCCs, and it is clear that the most robust part is the 22nF device.

Size	Cap nF	RC Network	Standards	1 Negative and 1 Positive Strike (AECQ200)					3 Negative and 3 Positive Strikes							
				6kV	8kV	12kV	16kV	25kV	6kV	8kV	12kV	15kV	16kV	25kV		
0603	4.7nF (50V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605									AD				
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605													
		330pF/2kΩ	ISO10605													
		330pF/330Ω	ISO10605													
	10nF (100V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605													
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605													
		330pF/2kΩ	ISO10605													
		330pF/330Ω	ISO10605													
	22nF (50V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605													AD
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605													
		330pF/2kΩ	ISO10605										AD			
		330pF/330Ω	ISO10605										AD			

Size	Cap nF	RC Network	Standards	5 Negative and 5 Positive Strikes						10 Negative and 10 Positive Strikes							
				6kV	8kV	12kV	15kV	16kV	25kV	6kV	8kV	12kV	15kV	16kV	25kV		
0603	4.7nF (50V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605				AD							AD			
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605											AD			
		330pF/2kΩ	ISO10605											AD			
		330pF/330Ω	ISO10605											AD			
	10nF (100V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605													AD	
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605														AD
		330pF/2kΩ	ISO10605														
		330pF/330Ω	ISO10605														
	22nF (50V)	150pF/2kΩ	AECQ200 (Classification)/ISO10605														AD
		150pF/330Ω	IEC61000-4-2(Test Level)/ISO10605														
		330pF/2kΩ	ISO10605														AD
		330pF/330Ω	ISO10605														AD

Table 2 - ESD Robustness Tests. "AD" stands for "Air Discharge."

## CASE STUDY

The following test setup describes an example ESD test performed on a 0603 ESD-safe MLCC. Not only has the ESD withstand level been measured, but also the maximum peak voltage across the capacitor. An additional load resistor of 33 kΩ has been used in this test setup representing the input impedance of the downstream circuit.

The following equipment and measurements were used for the test:

- PCB-board: FR4 PCB test board 2 layer, 1.5mm
- Load resistor: 33kΩ ±1%
- High voltage probe: P6015A (Tektronix)
- Oscilloscope (digital): MSO54-5-BW-2000 (Tektronix)
- 10 strikes (+/-) per unit.

The predetermined pass criteria for the test is:

- Tested components are within the electrical limits and with no mechanical defects after the tests.

# ELECTROSTATIC PROTECTION USING CERAMIC CAPACITORS

## CASE STUDY

As can be seen in the results in table 3, the MLCC capacitor safely reduces the applied ESD discharge by orders of magnitude. As long as the downstream components are rated to tolerate this reduced voltage, adequate protection can be realized in a simple, small, and cost-effective manner.

ESD performance test study							
tested component ESD31C103K4T2A-18 (0603,100V,10nF)							
Test Sequence	Discharge (10 strikes +/-)			Standards	Peak voltage		
	Type	Level (kV)	Network		Avg.	Min	Max
1	contact	15	C = 150pF, R = 330 Ohm	IEC61000-4-2	212	144	282
2	contact	8	C = 330pF, R = 2k Ohm	ISO10605	440	315	537
3	contact	15	C = 150pF, R = 2k Ohm	AECQ200/ISO10605	360	231	464

Table 3 - ESD-Safe performance test results

## CONCLUSION

The KYOCERA AVX ESD-Safe™ Series provides a wide range of ESD robust MLCC's tested according to the AECQ200, IEC61000-4-2, and ISO10605 standards. These capacitors offer an inexpensive alternative to protecting I/O lines where speed is not critical. In applications where MLCC's can not be used, it is recommended to simply use the more traditional Multilayer Varistor (MLV).

For more details please refer to [www.kyocera-avx.com](http://www.kyocera-avx.com) for a product portfolio and technical papers.



**NORTH AMERICA**  
Tel: +1 864-967-2150

**CENTRAL AMERICA**  
Tel: +55 11-46881960

**EUROPE**  
Tel: +44 1276-697000

**ASIA**  
Tel: +65 6286-7555

**JAPAN**  
Tel: +81 740-321250

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