

TECHNICAL PAPER

Low Inductance Capacitors for High-Speed Decoupling

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Abstract

Modern integrated circuits (IC's) consume power at rapidly varying rates due to the density of circuits on-board and the extreme speed at which they can operate. Power supplies are required to respond to these changes in load current while maintaining a constant operating voltage. This task is becoming increasingly difficult as the complexity of power distribution networks grows and printed circuit board (PCB) design requires optimization for parasitic inductance and capacitance.



LOW INDUCTANCE CAPACITORS FOR HIGH-SPEED DECOUPLING

AN OVERVIEW OF DECOUPLING CAPACITORS

Modern integrated circuits (IC's) consume power at rapidly varying rates due to the density of circuits on-board and the extreme speed at which they can operate. Power supplies are required to respond to these changes in load current while maintaining a constant operating voltage. This task is becoming increasingly difficult as the complexity of power distribution networks grows and printed circuit board (PCB) design requires optimization for parasitic inductance and capacitance. Therefore, any power supply performance slack must be absorbed by the all-too-common decoupling capacitor. As shown in Figure 1, a decoupling capacitor is simply an additional parallel capacitance that provides a stable voltage and source of current when the main power supply is unable to adjust quickly enough or is too far away to properly function.

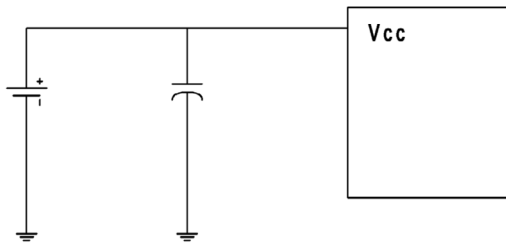


Figure 1 - Power supply, decoupling capacitor, and integrated circuit

Unfortunately, the idealized notion of a capacitor as an instantaneously available energy source is far from the truth at higher frequencies. As shown in Figure 2, physical capacitors present a parasitic equivalent series inductance (ESL) and equivalent series resistance (ESR) in addition to the bulk capacitance.

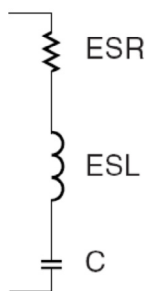


Figure 2 - Realistic capacitor equivalent circuit model

As the operating frequency of IC's continues to rise, these parasitic elements become of greater significance when considering a capacitor for decoupling purposes. As the frequency increases, the AC impedance of the equivalent circuit model drops, and the capacitive component loses dominance. At a certain point, the inductive and capacitive components are equivalent, and the inductance becomes dominant above this frequency. This crossover point is known as the self-resonant frequency and is visible in Figure 3, showing the frequency response of 100 nF, 0603 ceramic capacitors.

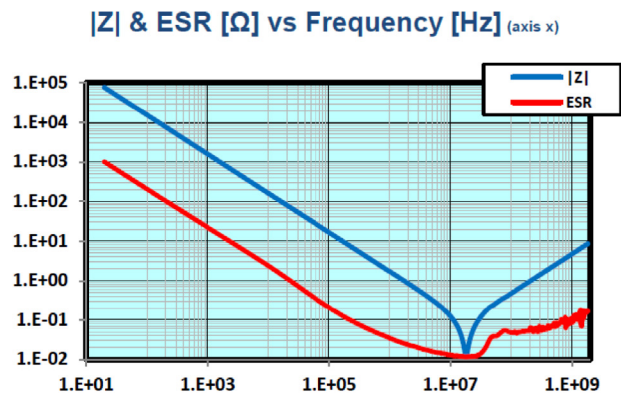


Figure 3 - Capacitor frequency response example

At low frequencies, decoupling performance may be as simple as just adding an adequately sized multi-layer ceramic capacitor (MLCC) as close as possible to the target IC. However, achieving decoupling performance at high frequencies is a much more complex and nuanced problem.

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DECOUPLING FOR HIGH-PERFORMANCE CIRCUITS

For high-performance circuits, proper decoupling requires the designer to consider the frequency demands of the load, the frequency response of the capacitor, and the overall layout and routing of the PCB. It is also common to discover that a single capacitor is inadequate, and instead, an array of capacitors of different values and constructions must be employed. Tantalum or aluminum electrolytic devices are preferable for low frequency and high capacitance. For high frequency and low ESL, multiple parallel ceramics are typically used. For n discrete devices in parallel, the capacitance is increased to nC , the inductance is decreased to ESL/n , and the resistance is decreased to ESR/n . The self-resonance frequency remains the same as the original single capacitor.

The positioning of these capacitors is also of utmost importance. The term “decoupling diameter” is often used to describe the maximum distance from the target IC that a particular capacitor can serve as an effective decoupling component. When considering PCB trace length and inductance, the farther away from the target IC a capacitor is, the lower the frequency it can effectively respond to. As such, the decoupling diameter of a particular capacitor is conceptually visualized as the phase difference between the power supply noise pulses and the capacitor’s offsetting currents. Based on experience, the distance of decoupling diameter should be controlled within $\frac{\lambda}{40} - \frac{\lambda}{50}$.

The high-frequency capacitor array should be placed physically close to the IC, considering decoupling diameter and MLCC bulk capacitance. An example is shown in Figure 4, where a complex capacitor array is included on the actual CPU package for decoupling high-frequency power draws.

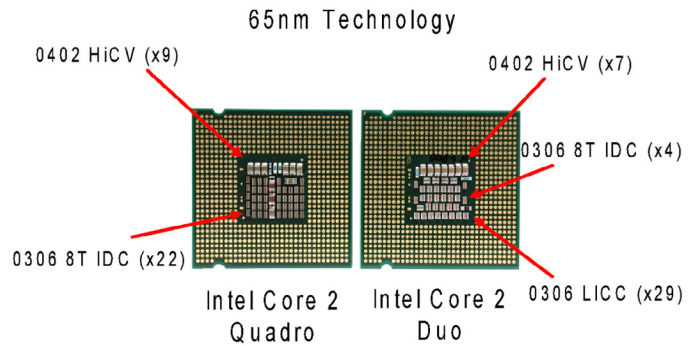


Figure 4 - Intel CPU with low ESL decoupling array

In addition to placement, the actual routing and via hole design should be considered to minimize inductance. The inductance of a through-hole is shown in the equation below:

$$L = 5.08h \left[\ln \left(\frac{4h}{d} \right) + 1 \right]$$

Equation 1 - Inductance of a PCB through-hole

- L: the inductance of through-hole, unit nH
- h: the length of the through-hole, unit inch
- d: the diameter of the through-hole, unit inch

Figure 5 shows that the actual via placement relative to the PCB trace also affects inductance. The optimal configuration is to place the via within the actual capacitor pad and eliminate any length of trace all together.

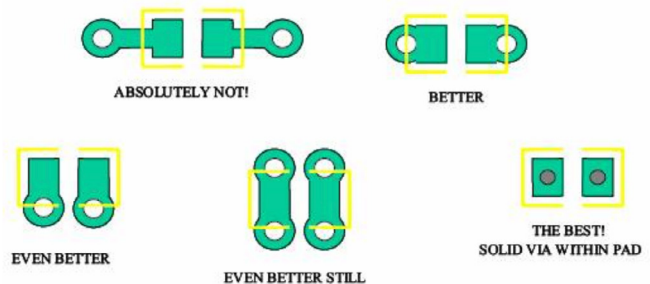


Figure 5 - Via placement for low inductance

LOW INDUCTANCE CAPACITORS FOR HIGH-SPEED DECOUPLING

LOW INDUCTANCE CAPACITOR FAMILIES

While optimization of PCB layout and capacitor array values is important, the choice of the actual capacitor construction can yield the greatest performance benefit. Unfortunately, this requires a complex trade-off analysis concerning size, cost, performance, and availability. Several low ESL capacitor families are available from KYOCERA AVX, including low inductance chip, feedthrough, interdigitated, and land grid array.

Low Inductance Chip Capacitors

A Low Inductance Chip Capacitor (LICC), sometimes referred to as Reverse Geometry Capacitor (RGC), has its terminations on the longer sides of its rectangular shape. This difference is shown in Figure 6. By reducing the distance between the terminations, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL than a 0603. The reduction in ESL varies by EIA size. However, ESL is typically reduced by 60% or more with an LICC versus a standard MLCC.

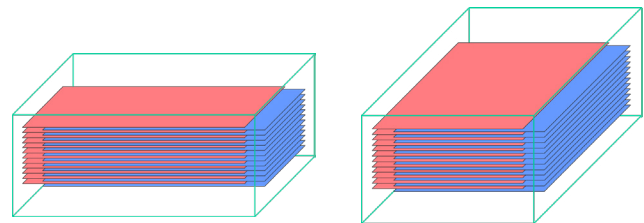


Figure 6 - Traditional MLCC (left) and reverse geometry for low ESL (right)

Feedthrough Capacitors

Also known as three-terminal capacitors, feedthrough capacitors are constructed so that the input and output inductance cancel each other out, and a dedicated low inductance path to ground is guaranteed. Figure 7 shows a common feedthrough structure and the equivalent circuit model.

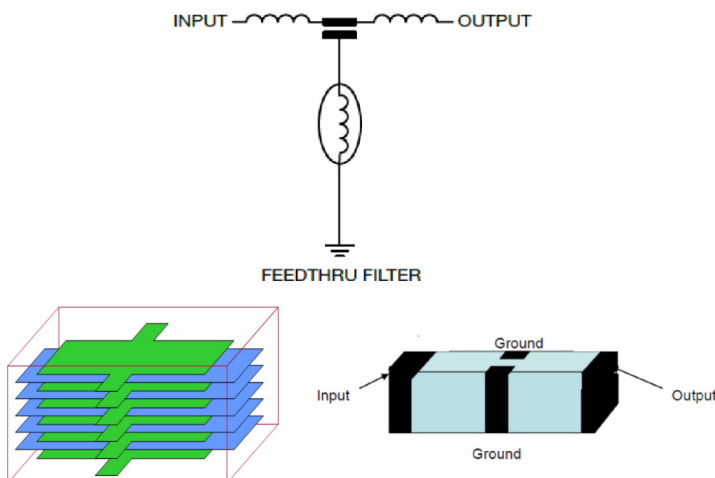


Figure 7 - Feedthrough capacitor internal structure and equivalent circuit

Figure 8 presents the frequency response of a feedthrough device compared to several other capacitor structures. The inductance at high frequency is reduced while only marginally affecting the PCB complexity and area.

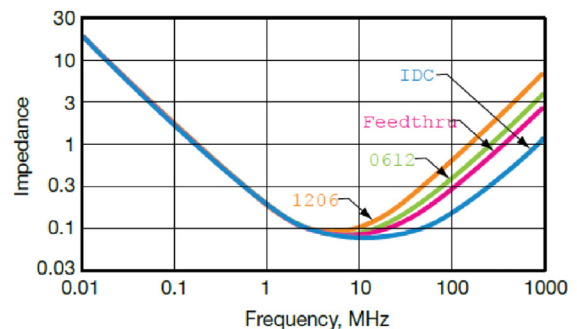


Figure 8 - Feedthrough capacitor frequency response compared to 1206, 0612, and IDC devices

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LOW INDUCTANCE CAPACITOR FAMILIES

Interdigitated Capacitors

Interdigitated capacitors (IDC) are a specialized capacitor family used to replace a capacitor array for package level and board level decoupling applications. These capacitors offer the lowest ESL while simultaneously reducing PCB space requirements compared to an equivalent MLCC array, as shown in Figure 9.

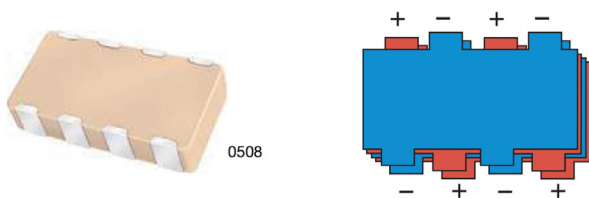


Figure 9 - Interdigitated capacitor structure

A representative frequency response is shown in Figure 10, where the IDC exhibits a lower ESL compared to an MLCC by more than an order of magnitude.

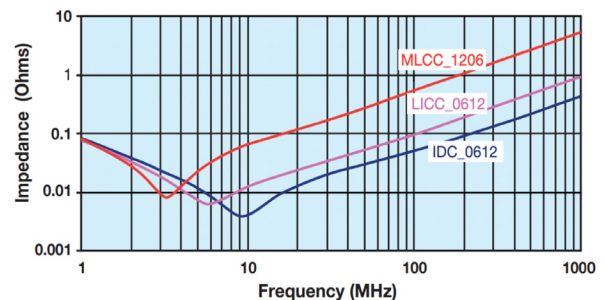


Figure 10 - IDC frequency response compared to LICC and MLCC

Land Grid Array Capacitors

Land grid array (LGA) capacitors offer comparable low ESL performance to IDC devices but use an advanced manufacturing process to orient the inner terminals vertically, thus reducing the number of PCB terminations.

As a result, PCB area requirements are minimized, and overall capacitor density can be increased. The internal structure of the LGA device is shown in Figure 11.

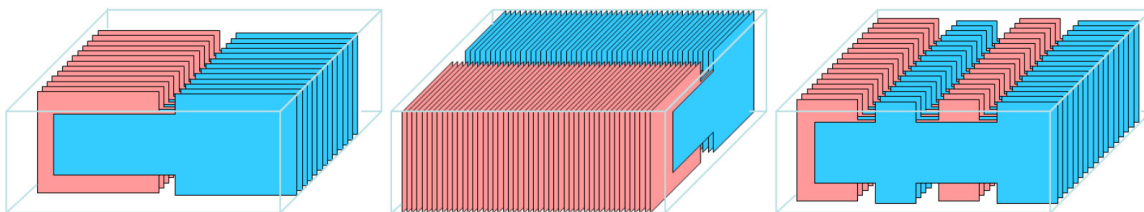


Figure 11 - LGA capacitor internal structure

ESL CAPACITORS FOR HIGH-FREQUENCY DECOUPLING

Designing a power delivery network for high-performance IC's requires careful layout, selection, and routing of the decoupling capacitors. Traditional electrolytics and MLCCs can be used for low to mid-frequency bands. For high frequencies, engineers must employ more advanced techniques and devices.

KYOCERA AVX offers a variety of low ESL capacitors for high-frequency decoupling of board-level and package-level circuits.

For more information on KYOCERA AVX capacitors, visit www.kyocera-avx.com.



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