

AVX
Low Inductance Capacitors

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Introduction

As switching speeds increase and pulse rise times decrease the need to reduce inductance becomes a serious limitation for improved system performance. Even the decoupling capacitors, that act as a local energy source, can generate unacceptable voltage spikes: $V = L (di/dt)$. Thus, in high speed circuits, where di/dt can be quite large, the size of the voltage spike can only be reduced by reducing L .

Figure 1 displays the evolution of ceramic capacitor toward lower inductance designs over the last few years. AVX has been at the forefront in the design and manufacture of these newer more effective capacitors.

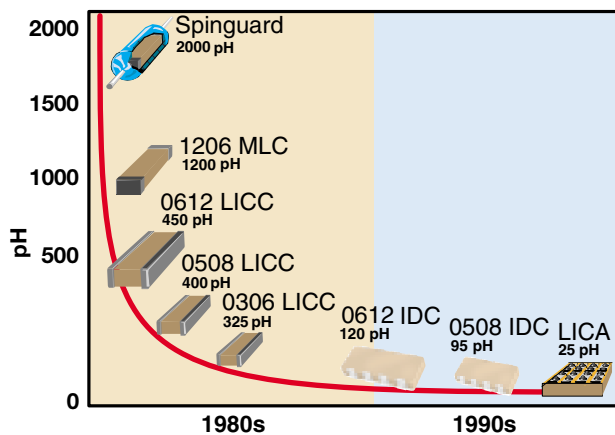


Figure 1. The evolution of Low Inductance Capacitors at AVX (values given for a 100 nF capacitor of each style)

LOW INDUCTANCE CHIP CAPACITORS

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes. Thus a 1210 chip size has lower inductance than a 1206 chip. This design improvement is the basis of AVX's low inductance chip capacitors, LI Caps, where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612 as demonstrated in Figure 2. In the same manner, an 0805 becomes an 0508 and 0603 becomes an 0306. This results in a reduction in inductance from around 1200 pH for conventional MLC chips to below 400 pH for Low Inductance Chip Capacitors. Standard designs and performance of these LI Caps are given on pages 29 and 30.

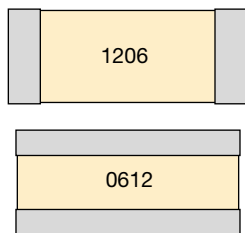
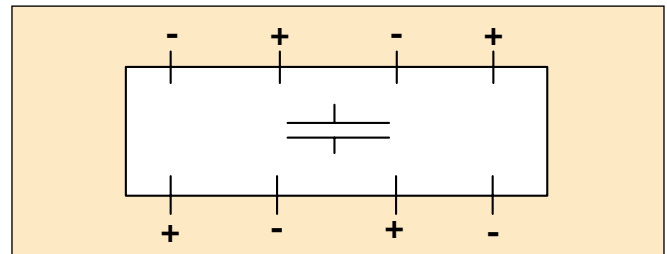


Figure 2. Change in aspect ratio: 1206 vs. 0612

INTERDIGITATED CAPACITORS

Multiple terminations of a capacitor will also help in reducing the parasitic inductance of the device. The IDC is such a device. By terminating one capacitor with 8 connections the ESL can be reduced even further. The measured inductance of the 0612 IDC is 120 pH, while the 0508 comes in around 95 pH. These FR4 mountable devices allow for even higher clock speeds in a digital decoupling scheme. Design and product offerings are shown on pages 31 and 32.



LOW INDUCTANCE CHIP ARRAYS (LICA®)

Further reduction in inductance can be achieved by designing alternative current paths to minimize the mutual inductance factor of the electrodes (Figure 3). This is achieved by AVX's LICA® product which was the result of a joint development between AVX and IBM. As shown in Figure 4, the charging current flowing out of the positive plate returns in the opposite direction along adjacent negative plates. This minimizes the mutual inductance.

The very low inductance of the LICA capacitor stems from the short aspect ratio of the electrodes, the arrangement of the tabs so as to cancel inductance, and the vertical aspect of the electrodes to the mounting surface.

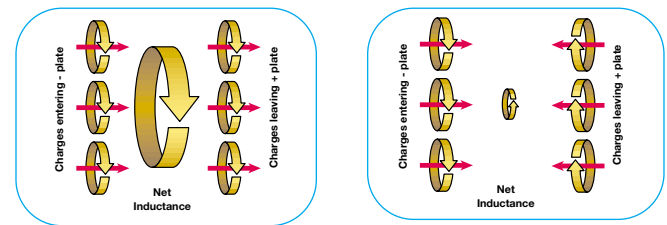


Figure 3. Net Inductance from design. In the standard Multilayer capacitor, the charge currents entering and leaving the capacitor create complementary flux fields, so the net inductance is greater. On the right, however, if the design permits the currents to be opposed, there is a net cancellation, and the inductance is much lower.

Low Inductance Capacitors



Introduction

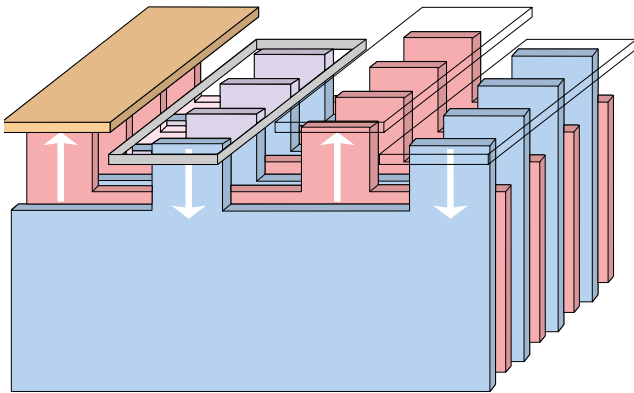


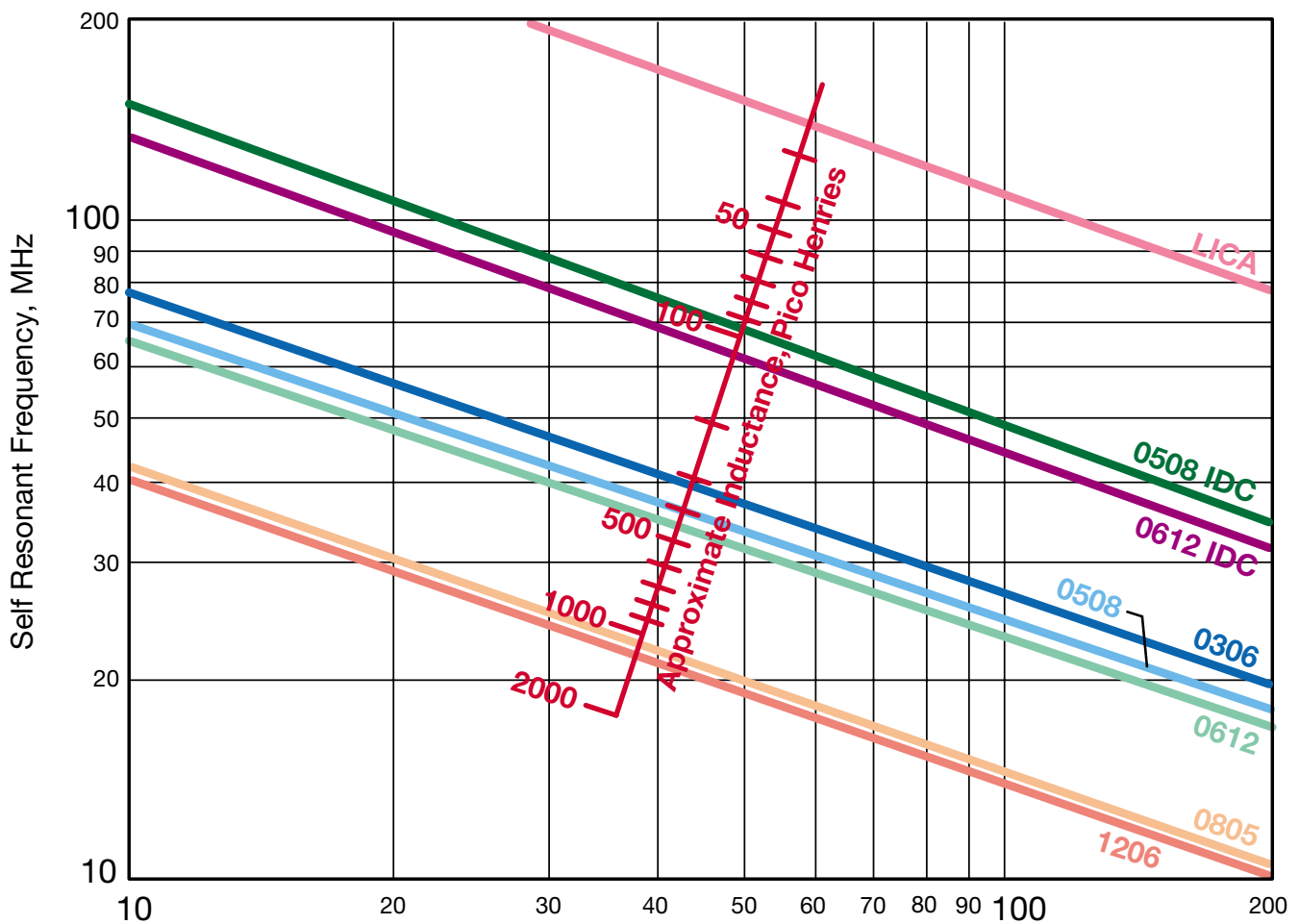
Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 50 pH, causing the self-resonance to be above 100 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 33 and 34.

Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.



Self Resonant Frequencies vs. Capacitance and Capacitor Design

Figure 5



Low Inductance Capacitors

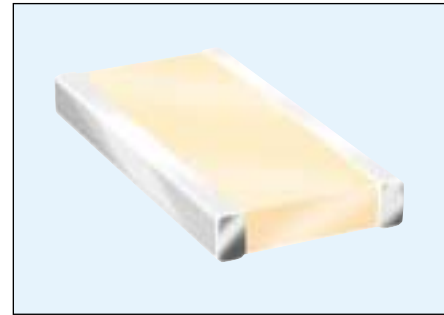


0612/0508/0306 LICC (Low Inductance Chip Capacitors)

GENERAL DESCRIPTION

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes.

Thus a 1210 chip size has a lower inductance than a 1206 chip. This design improvement is the basis of AVX's Low Inductance Chip Capacitors (LICC), where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612, in the same manner, an 0805 becomes an 0508, an 0603 becomes an 0306. This results in a reduction in inductance from the 1nH range found in normal chip capacitors to less than 0.4nH for LICCs. Their low profile is also ideal for surface mounting (both on the PCB and on IC package) or inside cavity mounting on the IC itself.



HOW TO ORDER

0612

Size
0306
0508
0612

Z

Voltage
6 = 6.3V
Z = 10V
Y = 16V
3 = 25V

D

Dielectric
C = X7R
D = X5R

105

Capacitance Code
2 Sig. Digits +
Number of Zeros

M

Capacitance Tolerance
K = $\pm 10\%$
M = $\pm 20\%$

A

Failure Rate
A = N/A

T

Terminations
T = Plated Ni
and Solder

2

Packaging Available
2 = 7" Reel
4 = 13" Reel

A*

Thickness
Thickness
mm (in)
0.56 (0.022)
0.61 (0.024)
0.76 (0.030)
1.02 (0.040)
1.27 (0.050)

PERFORMANCE CHARACTERISTICS

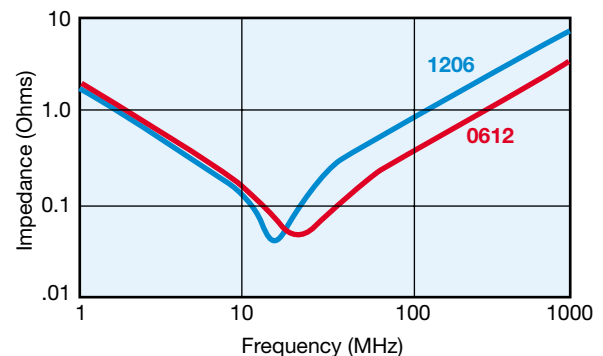
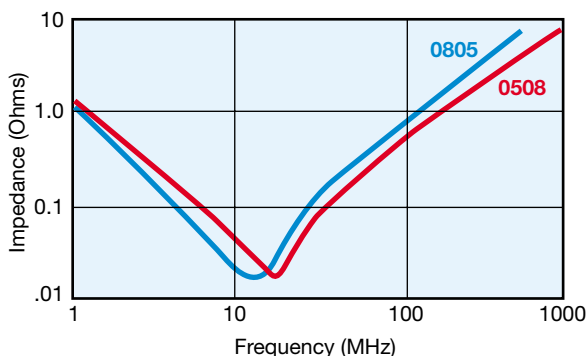
Capacitance Tolerances	K = $\pm 10\%$; M = $\pm 20\%$
Operation Temperature Range	X7R = -55°C to +125°C; X5R = -55°C to +85°C
Temperature Coefficient	$\pm 15\%$ (0VDC)
Voltage Ratings	6.3, 10, 16, 25 VDC
Dissipation Factor	6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max; 25V = 3.0% max
Insulation Resistance (@+25°C, RVDC)	100,000M Ω min, or 1,000M Ω per μ F min., whichever is less

TYPICAL INDUCTANCE

Package Style	Measured Inductance (pH)
1206 MLCC	1200
0612 LICC	450
0508 LICC	400
0306 LICC	325

*Note: See Range Chart for Codes

TYPICAL IMPEDANCE CHARACTERISTICS



Low Inductance Capacitors



0612/0508/0306 LICC (Low Inductance Chip Capacitors)

SIZE	0306		0508			0612			
Length	MM	0.81 ± 0.15 (0.032 ± 0.006)	1.27 ± 0.25 (0.050 ± 0.010)			1.60 ± 0.25 (0.063 ± 0.010)			
Width	MM	1.60 ± 0.15 (0.063 ± 0.006)	2.00 ± 0.25 (0.080 ± 0.010)			3.20 ± 0.25 (0.126 ± 0.010)			
WVDC		10 16	6.3 10 16 25	6.3 10 16 25	6.3 10 16 25	6.3 10 16 25	6.3 10 16 25	6.3 10 16 25	6.3 10 16 25
CAP (uF) and Thickness									
0.010									
0.015									
0.022									
0.047									
0.068									
0.10									
0.15									
0.22									
0.47									
0.68									
1.0									
1.5									
2.2									
3.3									

Consult factory for additional requirements

Solid = X7R = X5R

mm (in.)

0306	
Code	Thickness
A	0.61 (0.024)

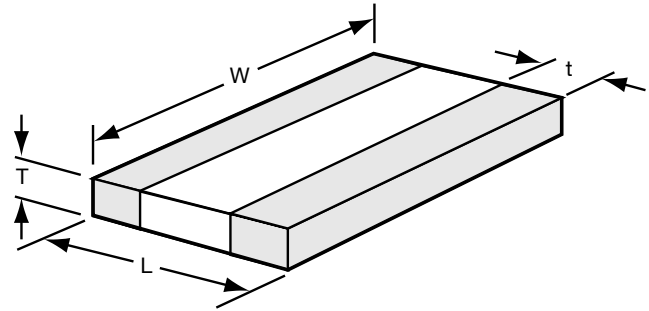
mm (in.)

0508	
Code	Thickness
S	0.56 (0.022)
V	0.76 (0.030)
A	1.02 (0.040)

mm (in.)

0612	
Code	Thickness
S	0.56 (0.022)
V	0.76 (0.030)
W	1.02 (0.040)
A	1.27 (0.050)

PHYSICAL DIMENSIONS AND PAD LAYOUT



PHYSICAL CHIP DIMENSIONS

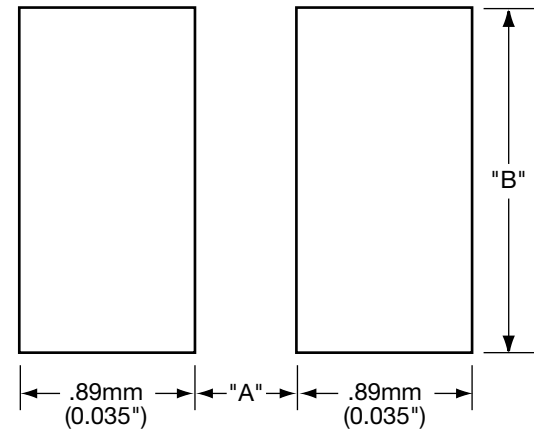
mm (in)

	L	W	t
0612	1.60 ± 0.25 (0.063 ± 0.010)	3.20 ± 0.25 (0.126 ± 0.010)	0.13 min. (0.005 min.)
0508	1.27 ± 0.25 (0.050 ± 0.010)	2.00 ± 0.25 (0.080 ± 0.010)	0.13 min. (0.005 min.)
0306	0.81 ± 0.15 (0.032 ± 0.006)	1.60 ± 0.15 (0.063 ± 0.006)	0.13 min. (0.005 min.)

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS

	A	B
0612	0.76 (0.030)	3.05 (0.120)
0508	0.51 (0.020)	2.03 (0.080)
0306	0.31 (0.012)	1.52 (0.060)



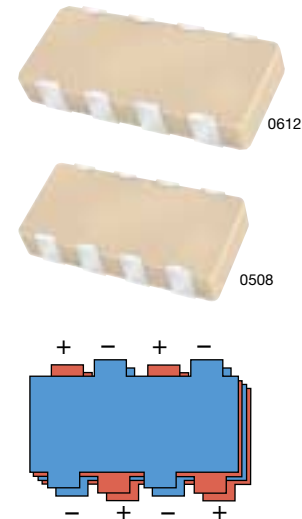
Low Inductance Capacitors



0612/0508 IDC (InterDigitated Capacitors)

GENERAL DESCRIPTION

- Very low equivalent series inductance (ESL), surface mountable, high speed decoupling capacitor in 0612 and 0508 case size.
- Measured inductances of 120 pH (for 0612) and 95 pH (for 0508) are the lowest in the FR4 mountable device family.
- Opposing current flow creates opposing magnetic fields. This causes the fields to cancel, effectively reducing the equivalent series inductance.
- Perfect solution for decoupling high speed microprocessors by allowing the engineers to lower the power delivery inductance of the entire system through the use of eight vias.
- Overall reduction in decoupling components due to very low series inductance and high capacitance.



HOW TO ORDER

W	3	L	1	6	D	225	M	A	T	3	A
Style	Case Size	Low Inductance	Number of Caps	Voltage	Dielectric	Capacitance Code	Capacitance Tolerance	Failure Rate	Termination	Packaging Available	Thickness
	2 = 0508 3 = 0612	ESL = 95pH ESL = 120pH		4 = 4V 6 = 6.3V Z = 10V Y = 16V	C = X7R D = X5R	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	A = N/A	T = Plated Ni and Solder	1=7" Reel 3=13" Reel	Max. Thickness mm (in.) A=0.95 (0.037) S=0.55 (0.022)

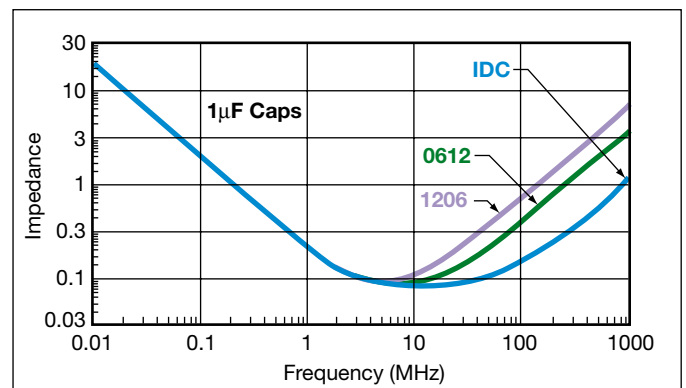
PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	±20% Preferred (10% Available)
Operation Temperature Range	X7R = -55°C to +125°C; X5R = -55°C to +85°C
Temperature Coefficient	±15% (OVDC)
Voltage Ratings	4, 6.3, 10, 16 VDC
Dissipation Factor	4V, 6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max
Insulation Resistance (@+25°C, RVDC)	100,000MΩ min, or 1,000MΩ per μF min., whichever is less

Dielectric Strength	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
CTE (ppm/C)	12.0
Thermal Conductivity	4-5W/M K
Terminations Available	Plated Nickel and Solder
Max. Thickness	0.037" (0.95mm)

TYPICAL ESL AND IMPEDANCE

Package Style	Measured Inductance (pH)
1206 MLCC	1200
0612 LICC	450
0612 IDC	120
0508 IDC	95



Low Inductance Capacitors

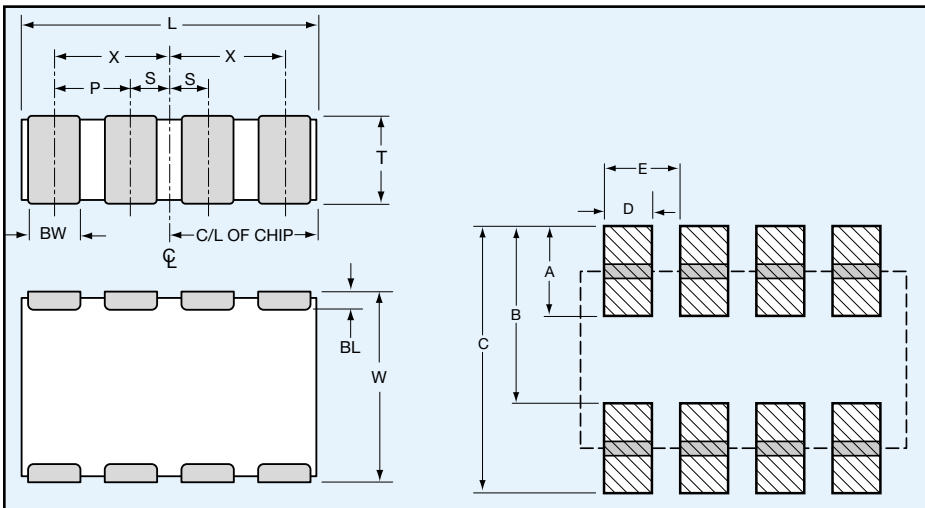
0612/0508 IDC (InterDigitated Capacitors)

SIZE	Thin 0508				0508				Thin 0612				0612				
Length	MM (in.)	2.03 ± 0.20 (0.080 ± 0.008)				2.03 ± 0.20 (0.080 ± 0.008)				3.20 ± 0.20 (0.126 ± 0.008)				3.20 ± 0.20 (0.126 ± 0.008)			
Width	MM (in.)	1.27 ± 0.20 (0.050 ± 0.008)				1.27 ± 0.20 (0.050 ± 0.008)				1.60 ± 0.20 (0.063 ± 0.008)				1.60 ± 0.20 (0.063 ± 0.008)			
Terminal Pitch	MM (in.)	0.508 REF 0.020 REF				0.508 REF 0.020 REF				0.76 REF 0.030 REF				0.76 REF 0.030 REF			
Thickness	MM (in.)	0.55 MAX. (0.022) MAX.				0.95 MAX. (0.037) MAX.				0.55 MAX. (0.022) MAX.				0.95 MAX. (0.037) MAX.			
Inductance (pH)		95				95				120				120			
WVDC		4	6.3	10	16	4	6.3	10	16	4	6.3	10	16	4	6.3	10	16
CAP (uF) and Thickness																	
0.047																	
0.068																	
0.10																	
0.22																	
0.33																	
0.47																	
0.68																	
1.0																	
1.5																	
2.2																	
3.3																	

Consult factory for additional requirements

= X7R
 = X5R

PHYSICAL DIMENSIONS AND PAD LAYOUT



PHYSICAL CHIP DIMENSIONS millimeters (inches)

0612

L	W	T	BW	BL	P	X	S
3.20 ± 0.20 (0.126 ± 0.008)	1.60 ± 0.20 (0.063 ± 0.008)	1.22 MAX. (0.048 MAX.)	0.41 ± 0.10 (0.016 ± 0.004)	0.18 ^{+0.25} _{-0.08} 0.07 ^{+0.010} _{-0.003}	0.76 REF (0.030 REF)	1.14 ± 0.10 (0.045 ± 0.004)	0.38 ± 0.10 (0.015 ± 0.004)

0508

L	W	T	BW	BL	P	X	S
2.03±0.20 (0.080±0.008)	1.27±0.20 (0.050±0.008)	0.965 MAX. (0.038 MAX.)	0.254±0.10 (0.010±0.004)	0.18 ^{+0.25} _{-0.08} 0.07 ^{+0.010} _{-0.003}	0.508 REF (0.020 REF)	0.76±0.10 (0.030±0.004)	0.254±0.10 (0.010±0.004)

PAD LAYOUT DIMENSIONS

0612

A	B	C	D	E
0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.46 (0.018)	0.79 (0.030)

0508

A	B	C	D	E
0.64 (0.025)	1.27 (0.050)	1.91 (0.075)	0.28 (0.011)	0.51 (0.020)

Low Inductance Capacitors

LICA® (Low Inductance Decoupling Capacitor Arrays)



LICA® arrays utilize up to four separate capacitor sections in one ceramic body (see Configurations and Capacitance Options). These designs exhibit a number of technical advancements:

Low Inductance features—

- Low resistance platinum electrodes in a low aspect ratio pattern
- Double electrode pickup and perpendicular current paths
- C4 “flip-chip” technology for minimal interconnect inductance

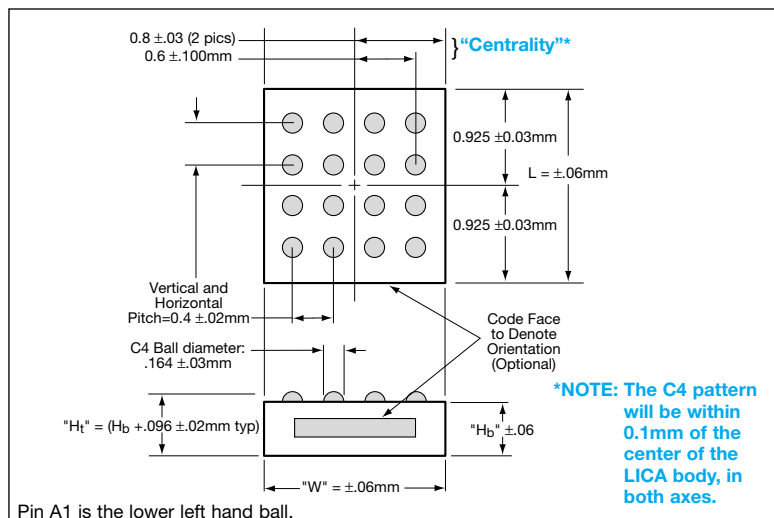
HOW TO ORDER

LICA	3	T	183	M	3	F	C	4	A	A
Style & Size	Voltage 25V = 3 50V = 5	Dielectric T = T55T S = High K T55T	Cap/Section (EIA Code) 102 = 1000 pF 103 = 10 nF 104 = 100 nF	Capacitance Tolerance M = ±20% P = GMV	Height Code 1 = 0.875mm 3 = 0.650mm 5 = 1.100mm 7 = 1.600mm	Termination F = C4 Solder Balls- 97Pb/3Sn P = Cr-Cu-Au N = Cr-Ni-Au X = None	Reel Packaging M = 7" Reel R = 13" Reel 6 = 2"x2" Waffle Pack 8 = 2"x2" Black Waffle Pack 7 = 2"x2" Waffle Pack w/ termination facing up A = 2"x2" Black Waffle Pack w/ termination facing up C = 4"x4" Waffle Pack w/ clear lid	# of Caps/Part 1 = one 2 = two 4 = four	Inspection Code A = Standard B = Established Reliability Testing	Code Face A = Bar B = No Bar C = Dot, S55S Dielectrics

TABLE 1

Typical Parameters	T55T	Units
Capacitance, 25°C	Co	Nanofarads
Capacitance, 55°C	1.4 x Co	Nanofarads
Capacitance, 85°C	Co	Nanofarads
Dissipation Factor 25°	12	Percent
DC Resistance	0.2	Ohms
IR (Minimum @25°)	2.0	Megaohms
Dielectric Breakdown, Min	500	Volts
Thermal Coefficient of Expansion	8.5	ppm/°C 25-100°
Inductance: (Design Dependent)	15 to 120	Pico-Henries
Frequency of Operation	DC to 5 Gigahertz	
Ambient Temp Range	-55° to 125°C	

C4 AND PAD DIMENSIONS



Code (Body Height)	Width (W)	Length (L)	Height Body (H _b)
1	1.600mm	1.850mm	0.875mm
3	1.600mm	1.850mm	0.650mm
5	1.600mm	1.850mm	1.100mm
7	1.600mm	1.850mm	1.600mm

TERMINATION OPTIONS

C4 SOLDER (97% Pb/3% Sn) BALLS



TERMINATION OPTION P OR N

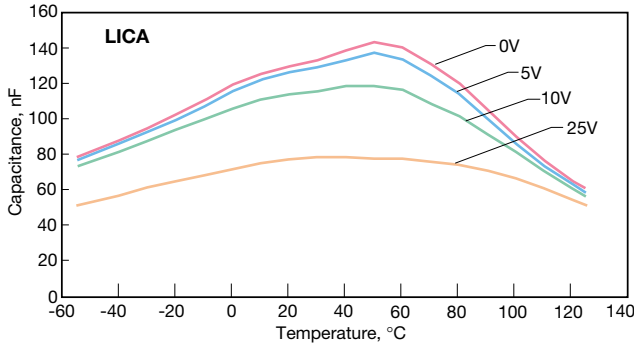


Low Inductance Capacitors

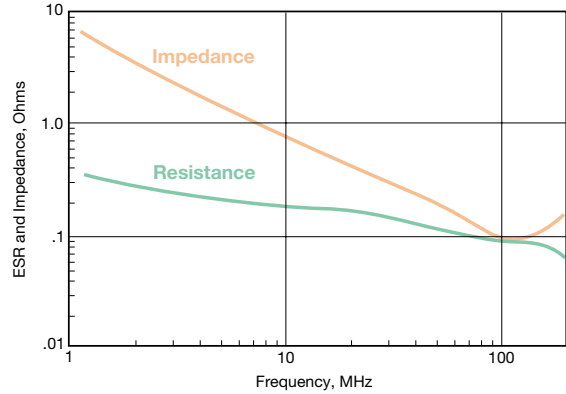


LICA® (Low Inductance Decoupling Capacitor Arrays)

LICA® TYPICAL PERFORMANCE CURVES



Effect of Bias Voltage and Temperature on a 130 nF LICA® (T55T)

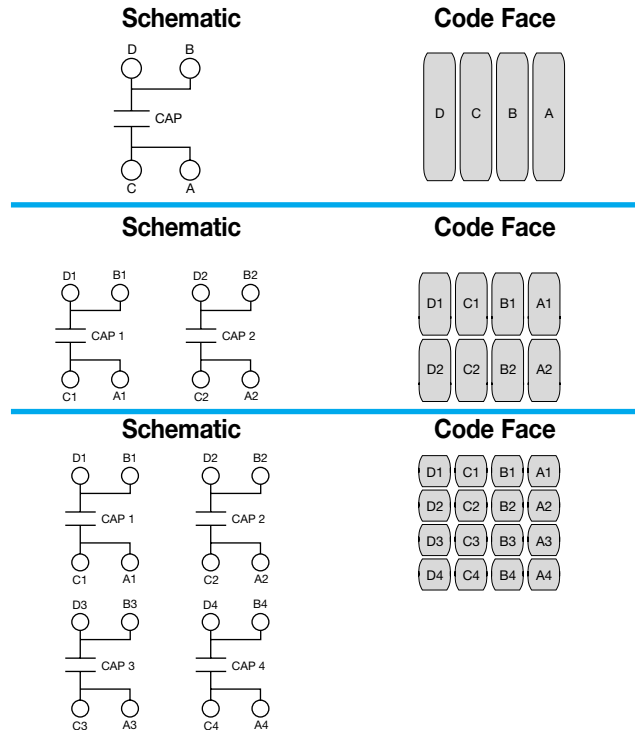


Impedance vs. Frequency

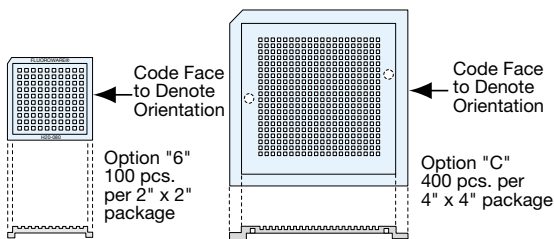
LICA VALID PART NUMBER LIST

Part Number	Voltage	Thickness (mm)	Capacitors per Package
LICA3T183M3FC4AA	25	0.650	4
LICA3T143P3FC4AA	25	0.650	4
LICA3T134M1FC1AA	25	0.875	1
LICA3T104P1FC1AA	25	0.875	1
LICA3T253M1FC4AA	25	0.875	4
LICA3T203P1FC4AA	25	0.875	4
LICA3T204M5FC1AA	25	1.100	1
LICA3T164P5FC1AA	25	1.100	1
LICA3T304M7FC1AB	25	1.600	1
LICA3T244P7FC1AB	25	1.600	1
LICA5T802M1FC4AB	50	0.875	4
LICA5T602P1FC4AB	50	0.875	4
Extended Range			
LICA3T104M3FC1A	25	0.650	1
LICA3T803P3FC1A	25	0.650	1
LICA3T503M3FC2A	25	0.650	2
LICA3T403P3FC2A	25	0.650	2
LICA3S213M3FC4A	25	0.650	4

CONFIGURATION



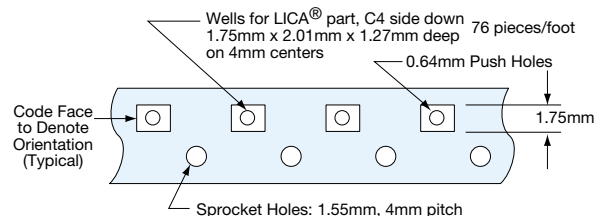
WAFFLE PACK OPTIONS FOR LICA®



Note: Standard configuration is Termination side down

LICA® PACKAGING SCHEME "M" AND "R"

8mm conductive plastic tape on reel:
 "M"=7" reel max. qty. 3,000, "R"=13" reel max. qty. 8,000



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DECOUPLING: BASICS

*By Arch Martin
AVX Corporation
Myrtle Beach, SC*

This paper discusses the characteristics of multilayer ceramic capacitors in decoupling applications and compares their performance with other types of decoupling capacitors. A special high-frequency test circuit is described and the results obtained using various types of capacitors are shown.

<http://www.avxcorp.com/docs/techinfo/dcpibsc.pdf>

FUNCTIONAL TESTING OF DECOUPLING CAPACITORS FOR DYNAMIC RAMs

*By Arch G. Martin Ward Parkinson
AVX Corporation Micron Technology, Inc.
Myrtle Beach, SC Boise, Idaho*

Comparative performance of various types of distributed decoupling capacitors both with and without bulk tantalum capacitors is shown under actual operating conditions in a 64K dynamic RAM memory board designed especially for high-frequency in-use testing. Multilayer ceramic capacitors are shown to be effective and economical even without using bulk tantalum capacitors for decoupling.

<http://www.avxcorp.com/docs/techinfo/dynamic.pdf>

IMPROVED NOISE SUPPRESSION VIA MULTILAYER CERAMIC CAPACITORS (MLCs) IN POWER-ENTRY DECOUPLING

*By Arch G. Martin R. Kenneth Keenan
AVX Corporation TKC
Myrtle Beach, SC Pinellas Park, FL*

A new decoupling technique is proposed for surface mounted designs that recommends using 0.1 μF MLCs as the circuit-level decoupling capacitors and 1.0 μF to 10 μF MLCs in place of the tantalum as the board-level power-entry capacitor. This combination of MLCs on each PCB coupled with a single system

level tantalum or aluminum is probably an optimum arrangement; performance is enhanced, and cost is not increased.

<http://www.avxcorp.com/docs/techinfo/supvmlc.pdf>

INDUCTANCE MEASUREMENTS FOR MULTI-TERMINAL DEVICES

*By Ben Smith
AVX Corporation
801 17th Avenue South
Myrtle Beach, SC 29578*

New innovations in both the telecommunication industry as well as the computer industry have mandated a need for using low inductance capacitive devices in power supply decoupling applications. With this being the case, different concepts for the construction of these devices have recently been the key to the success of reaching inductances of less than 50pH. There is, however, a significant bottleneck to the new innovation process due to measurement techniques. Most of the newer devices are using techniques such as multi-path current flow, short length, and equal and opposite current injection techniques to achieve low inductance levels. Also, coupled with these new designs is the need for higher energy storage capabilities and thus more capacitance. All of these effects are presenting more complex tasks in the measurement process. This paper gives both a generic approach for measurement as well as an exact approach specifically for the Interdigitated (IDC) type devices.

<http://www.avxcorp.com/docs/techinfo/immtld.pdf>

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INTERCONNECT SCHEMES FOR LOW INDUCTANCE CERAMIC CAPACITORS

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As digital electronic systems continue to operate at higher and higher frequencies, the use of low inductance decoupling capacitors continues to increase. The parasitic inductance of the devices themselves is important, but the method used to connect the components to the system, such as printed circuit boards (PCB), is also a considerable factor. Adding inductance in the connection scheme can eliminate some of the effectiveness of the use of these low inductance elements. This paper will examine some of the different schemes utilized at the board level to minimize the loop inductance of the decoupling capacitors.

<http://www.avxcorp.com/docs/techinfo/intercs.pdf>

INTRODUCTION TO CHOOSING MLC CAPACITORS FOR BYPASS/DECOUPLING APPLICATIONS

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Methods to ensure *signal integrity* using decoupling capacitors have been the topic of many papers in the past as well as in the present. One can find equally many methods of decoupling as well. This paper will illustrate one of these established methods and introduce it in a *theoretical* sense using the most simplistic of terms. The paper will also describe the methods of the past (in slow speed systems) and the practices of the present (in high speed systems).

<http://www.avxcorp.com/docs/techinfo/mlcbypas.pdf>

LOW INDUCTANCE CAPACITORS FOR DIGITAL CIRCUITS

By John Galvagni
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Ceramic capacitors have become one of the limiting factors in digital circuits because of intrinsic characteristics such as equivalent series resistance and inductance. There are many things which could be done to mitigate that, and we describe some of those in this paper. AVX's DCAP capacitor, (developed with and for IBM) is used as a benchmark to show how much can be done to improve the situation. We compare and contrast that part to those currently available.

http://www.avxcorp.com/docs/techinfo/LI_TI.pdf

PARASITIC INDUCTANCE OF MULTILAYER CERAMIC CAPACITORS

By Jeff Cain, Ph.D.
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The parasitic inductance of multilayer ceramic capacitors (MLCCs) is becoming more important in the decoupling of high speed digital systems. There exists conflicting data and statements on the parasitic inductance of the MLCC. This work shows the measurement techniques of the inductance parameters, focusing mainly on the fixturing needed to accurately measure the chips. The effects of various compensation and calibration methods will also be demonstrated. A comprehensive table will be shown that includes the parasitic inductance for a range of MLCCs from 0402 through 1210.

New, more recent data supports the conclusions of this study, however they prove the original data in this article to be inaccurate. New data shown in this catalog is believed to be true but is subject to measure and test fixture accuracy.

<http://www.avxcorp.com/docs/techinfo/parasitic.pdf>

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PE SERIES CAPACITORS DECOUPLING AND/OR FILTERING

*By John D. Prymak
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Decoupling is a means of eliminating or reducing those elements which restrict high speed operations. Filtering is driven by two considerations – emission and susceptance. The noise generated in high speed digital operations may need to be reduced, to achieve accepted levels of emission to prevent interference with other systems. Also, the system itself may have its distinct level of noise tolerance which would require filtering selected inputs to maintain integrity of the logic circuit operations. The solution to a decoupling problem *may* assist filtering, and vice versa; but, the optimum solution to either is not the optimum solution for the other. The *PE* devices were originally designed for filtering, and then were later designed for decoupling. The application defines the requirement and the optimum design.

<http://www.avxcorp.com/docs/techinfo/peseries.pdf>

***So many electrons, so little time...* THE NEED FOR LOW INDUCTANCE CAPACITORS**

*By John Galvagni, Sara Randall, Paul Roughan
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High di/dt ratios, large current pulses over short times, are an inevitable part of today's fast electronic circuitry. They can cause high voltage spikes when passing through paths that have inductance. The task of the designer then, is to have high energies available, but not the associated voltage excursions, by reducing the total inductance. Eliminating wire bonds, reducing path lengths, and using low inductance components is the regimen. This paper describes the availability of capacitors that can go a long way to providing the

energies needed, but simultaneously, lower the intrinsic inductance it contributes. We will review the source of the inductance, the current components available, and other advances that will give the designer a more useful menu.

<http://www.avxcorp.com/docs/techinfo/needli.pdf>

THE EFFECTS OF ESR AND ESL IN DIGITAL DECOUPLING APPLICATIONS

*By Jeff Cain, Ph.D.
AVX Corporation*

It is common place for digital integrated circuits to operate at switching frequencies of 100 MHz and above, even at the circuit board level. As these frequencies continue to increase, the parasitic of the decoupling capacitors must be considered. A study on the effects of equivalent series resistance (ESR) and equivalent series inductance (ESL) in a typical digital decoupling application is presented. Utilizing SPICE, it can be shown that the ESR and ESL of chip capacitors can dramatically alter the voltage seen by the integrated circuit (IC) By changing the values of the parasitics and comparing the results to the ideal case for a variety of frequencies, some common decoupling design rules are formulated.

http://www.avxcorp.com/docs/techinfo/esr_esl.pdf



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